QP Code: RM23MTECH091 Reg. No | | | | | | | | | | | AY 23

GIET UNIVERSITY, GUNUPUR – 765022

M. Tech (Second Semester) Examinations, May – 2024

MPCEC2010 – System-On-Programmable Chip Design

(VLSI)

Time: 3 Hrs Maximum: 70 Marks

(The figures in the right hand margin indicate marks.)

PART – A **(2 x 10 = 20 Marks)**

Q.1. Answer all questions	CO#	Blooms Level
a. What does IP mean in VLSI?	CO2	K2
b. Explain the advantages of using IP blocks in FPGAs.	CO2	K1
c. Differentiate between emulation and FPGA prototyping.	CO1	K2
d. Define IP-based design.	CO1	K3
e. Describe a real-time processing operating system.	CO3	K2
f. Outline the structure of an RTOS.	CO3	K2
g. Identify the three major components of FPGA architecture.	CO4	K3
h. Define a peripheral interface and explain its role.	CO4	K1
i. Define SoC in testing.	CO2	K2
j. List the four layers of application architecture.	CO3	K1

PART – B **(10 x 5=50 Marks)**

Answer ***ANY FIVE*** questions	Marks	CO#	Blooms Level
2. a. Describe the instruction set architecture (ISA) comprehensively.	5	CO1	K3
b. Differentiate between a NoC and SoC chip clearly.	5	CO1	K2
3.a. Explain the principles of routing thoroughly.	5	CO2	K3
b. Explain the steps involved in IP life cycle management in detail.	5	CO2	K4
4. a. Briefly elucidate on IP and its various types concisely.	5	CO3	K5
b. Explain the SoC architecture of an FPGA in depth.	5	CO3	K3
5.a. Differentiate between a peripheral and an interface explicitly.	5	CO4	K3
b. Elaborate on the concept of core wrapper in DFT (Design for Testability) extensively.	5	CO4	K4
6. a. Provide a comprehensive overview of IEEE P1500 and its significance in chip testing.	5	CO2	K5
b. Discuss the concept of pipelining in processor architecture thoroughly.	5	CO2	K3
7.a. Describe the role and importance of cache memory in enhancing processor performance in detail.	5	CO1	K5

	b.	Explain the concept of clock domain crossing and its associated challenges in digital design thoroughly.	5	CO1 K4
8.	a.	Discuss the importance and various techniques of power management in SoC design comprehensively.	5	CO3 K3
	b.	Provide a detailed explanation of the role of interconnects in the performance of SoC designs.	5	CO4 K4

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