QP Code: RM23MTECH151 | Reg. No | | | | | | | | | | | AY 23

GIET UNIVERSITY, GUNUPUR – 765022

M. Tech (Second Semester) Examinations, May – 2024

MPEEC2043 - IC Technology

(ECE)

Time: 3 Hrs | Maximum: 70 Marks

(The figures in the right hand margin indicate marks.)

PART – A **(2 x 10 = 20 Marks)**

Q.1. Answer all questions	CO#	Blooms Level
a. What are the primary considerations in semiconductor technology trend analysis, and how do they impact the development of semiconductor devices?	CO1	K1
b. Explain the significance of clean rooms in semiconductor fabrication processes.	CO1	K2
c. What are the primary methods of deposition in semiconductor fabrication, and how do they differ?	CO2	K3
d. Explain the process of silicon oxidation, including the thermal oxidation process and the properties of silicon dioxide.	CO2	K2
e. Explain various etching techniques: wet chemical, dry physical, and reactive ion etching.	CO3	K1
f. Define lithography and its methods: photoreactive materials, electron beam, and ion beam.	CO3	K2
g. Discuss VLSI testing process: technology trends, test equipment, and test economics.	CO4	K3
h. Explain minority carrier lifetime and diffusion length in semiconductor materials.	CO4	K2
i. Explain SOI fabrication techniques: SIMOX, bonded SOI, and Smart Cut.	CO1	K1
j. What are the features of PD SOI and FD SOI device structures?	CO2	K2

PART – B **(10 x 5=50 Marks)**

Answer ***ANY FIVE*** questions	Marks	CO#	Blooms Level
2. a. Explain the impact of crystal defects on semiconductor device performance and the measures taken to minimize their effects.	5	CO1	K2
b. Explore the advantages of the float zone growth method in semiconductor fabrication and its common applications.	5	CO1	K3
3.a. Examine ion implantation techniques in semiconductor manufacturing, including penetration range, ion implantation systems, and process considerations for achieving desired doping profiles.	5	CO2	K4
b. Discuss the effects of implantation damage and annealing in ion implantation processes and evaluate methods for evaluating diffused layers in semiconductor devices.	5	CO2	K5
4. a. Detail CMOS process flow: N well, P-well, and Twin tub techniques in semiconductor manufacturing.	5	CO3	K3

b.	Discuss design rules, layout considerations, and contact types like buried and butting contacts in MOS-based circuits.	5	CO3	K3
5.a.	Describe semiconductor measurements: conductivity type, resistivity, and their significance in semiconductor characterization.	5	CO4	K2
b.	Explore advanced semiconductor measurements like Hall effect measurements, drift mobility, and their applications in device analysis.	5	CO4	K3
6. a.	Describe SOI fabrication techniques: SIMOX, bonded SOI, and Smart Cut, and their applications.	5	CO2	K4
b.	Evaluate the performance of bipolar junction transistors (BJT) and the advantages of bipolar processes and BiCMOS technology.	5	CO2	K5
7.a.	Explore GaAs technologies: MESFET, digital, MMIC, and optoelectronic devices, and their applications.	5	CO1	K3
b.	Discuss the advancements in GaAs technologies, such as MESFET, MMIC, and optoelectronic devices.	5	CO1	K3
8. a.	Compare wet chemical, dry physical, and dry chemical etching techniques used in semiconductor fabrication.	5	CO3	K2
b.	Evaluate reactive ion etching and ion beam techniques in semiconductor processing.	5	CO4	K3

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