QPC: RJ23MTECH083 | Reg. No | | | | | | | | | | | AY 23

GIET UNIVERSITY, GUNUPUR – 765022

M. Tech (First Semester) Examinations, January – 2024

MPCVL1020 – Digital IC Design

(VLSI Design)

Time: 3 hrs | Maximum: 70 Marks

(The figures in the right hand margin indicate marks.)

PART – A **(2 x 10 = 20 Marks)**

Q.1	Answer all questions	CO#	Blooms Level
a.	What are the components of the data path?	CO1	K1
b.	What are the characteristics of static CMOS inverter?	CO1	K2
c.	Which architecture is used to design circuit?	CO1	K2
d.	What is the dynamic characteristic of MOSFET?	CO2	K1
e.	What is the basic cell of static RAM?	CO3	K2
f.	What is a transparent latch?	CO2	K1
g.	What is the different logic gate used in CMOS?	CO1	K3
h.	What is the difference between dynamic and static latches?	CO4	K1
i.	What is the difference between static RAM and dynamic RAM.	CO3	K3
j.	What are the components of the data path?	CO4	K1

PART – B **(10 x 5=50 Marks)**

Answer ***ANY FIVE*** questions

		Marks	CO#	Blooms Level
2. a.	Provide detailed explanations for the following circuits: i) Data path circuit ii) Any one adder circuit.	5	CO1	K2
b.	Delve into the intricacies of ratioed circuits and dynamic circuit CMOS logic configurations.	5	CO1	K3
3.a.	What are the key considerations in designing the layout of an NMOS inverter, and how does it differ from the stick diagram?	5	CO2	K2
b.	Illustrate the stick diagram and layout of an NMOS inverter.	5	CO2	K4
4. a.	Elaborate on the working principle of an SRAM cell.	5	CO3	K2
b.	Write a brief note on the sequencing of dynamic circuits.	5	CO3	K2
5.a.	Describe the structure of a Booth multiplier and enumerate its advantages.	5	CO4	K1
b.	Explain the structure of a Booth multiplier and list its advantages.	5	CO4	K2

6. a.	Describe the operation and diverse applications of enhancement and depletion mode devices in electronic circuits.	5	CO2	K3
b.	Explain the concept of accumulation mode in semiconductor devices.	5	CO3	K2
7.a.	Describe the 6-transistor SRAM cell configuration.	5	CO2	K4
b.	Highlight the differences between a latch and a flip-flop.	5	CO2	K2
8. a.	Discuss the applications and challenges associated with sequencing dynamic circuits.	5	CO1	K3
b.	Evaluate the advantages and disadvantages of a latch in electronic circuits.	5	CO2	K2

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