QP Code: RM21BTECH439 | Reg. No | | | | | | | | | | | AY 21

GIET UNIVERSITY, GUNUPUR – 765022

B. Tech (Sixth Semester Regular) Examinations, May – 2024

21BECPC36001 – Digital VLSI Design

(ECE)

Time: 3 hrs | Maximum: 70 Marks

(The figures in the right hand margin indicate marks)

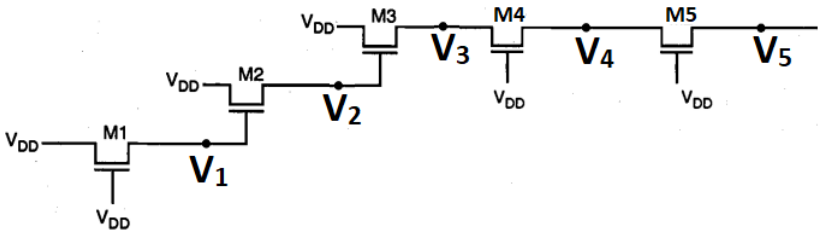
PART – A **(2 x 5 = 10 Marks)**

Q.1. Answer ***ALL*** questions	CO #	Blooms Level
a. Explain bottom up approach in VLSI design.	CO1	K1
b. Draw the symbol of enhancement and depletion type of n-MOSFET.	CO1	K2
c. What is parasitic capacitance in CMOS circuit?	CO2	K3
d. What is interconnect delay in VLSI circuit?	CO3	K3
e. Draw the nMOS pass transistor, and explain its working.	CO4	K3

PART – B **(15 x 4 = 60 Marks)**

Answer ***ALL*** questions	Marks	CO #	Blooms Level
2. a. What is oxidation and photolithography in semiconductor fabrication industry? Discuss the quality of oxide and method of photolithography.	7	CO1	K2
b. Explain top down approach for VLSI logic circuit design.	8	CO1	K3
(OR)			
c. What is stick diagram? Draw an enhancement type load (nMOS) inverter circuit and design its stick diagram.	7	CO1	K2
d. Explain each step of fabrication for n-MOSFET,	8	CO1	K3
3.a. Explain the working principle of p-MOSFET for different gate bias condition. Draw its cross-sectional view to explain its region of operation.	10	CO2	K4
b. What are the advantages of dynamic logic circuit?	5	CO2	K4
(OR)			
c. Calculate the threshold voltage V_{TH} at V_{SB} = 0, for a polysilicon gate n-channel MOSFET. Substrate doping density $N_A = 10^{16}$ cm^{-3}, polysilicon gate doping density $N_D = 2\times10^{20}$ cm^{-3}, gate oxide thickness t_{ox}= 500 Å, and oxide-interface fixed charge density $N_{ox} = 4\times10^{10}$ cm^{-2}.	10	CO2	K3
d. Explain CMOS inverter circuit with its real characteristics.	5	CO2	K4
4.a. Draw the clocked CMOS SR-latch circuit based on NAND gate and explain its function and write the corresponding truth table.	10	CO3	K4
b. Implement the Boolean expression (XY+CD+E)) by using enhancement nMOS type load.	5	CO3	K5
(OR)			
c. Draw the circuit diagram for CMOS D-Latch using transmission gate and explain its working.	10	CO3	K4

d.	What is transmission gate? Implement the Boolean expression $X\bar{Y}+XY$ using transmission gate.	5	CO3	K5
5.a.	What is voltage Bootstrapping. Explain bootstrapping technique by considering an inverter (with enhancement type nMOS load with unknown voltage Vx at gate terminal) circuit and find ratio of boot capacitor and source-to-substrate capacitance.	10	CO4	K5
b.	Observe the given circuit and find the voltage V_1, V_2, V_3, V_4, and V_5. Consider the threshold voltage for nMOS transistor M1, M2, M3, M4, and M5 as V_{TH1}, V_{TH2}, V_{TH3}, V_{TH4}, and V_{TH5} respectively.	5	CO4	K4



(OR)

c.	What is precharge and evaluate in Dynamic logic circuit? Using this technique, draw and explain the working of dynamic CMOS circuit for the Boolean expression $\overline{(A_1 \cdot A_2 \cdot A_3)+(B_1 \cdot B_2)}$.	10	CO4	K5
d.	What is domino CMOS logic? Explain with example.	5	CO4	K4

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