GIET UNIVERSITY, GUNUPUR – 765022

B. Tech (Fourth Semester - Regular) Examinations, May – 2024

22BELPC24004 – Analog and Digital Circuits

(EE & EEE)

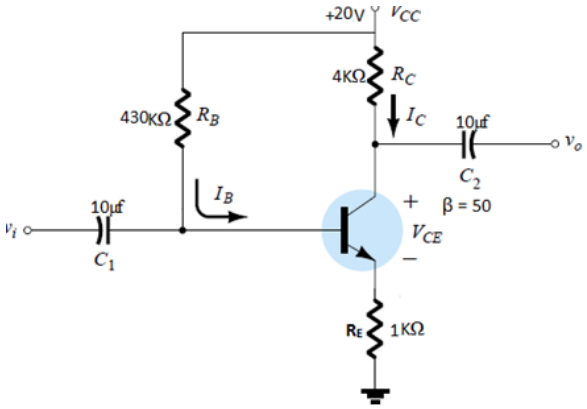
Time: 3 hrs Maximum: 70 Marks

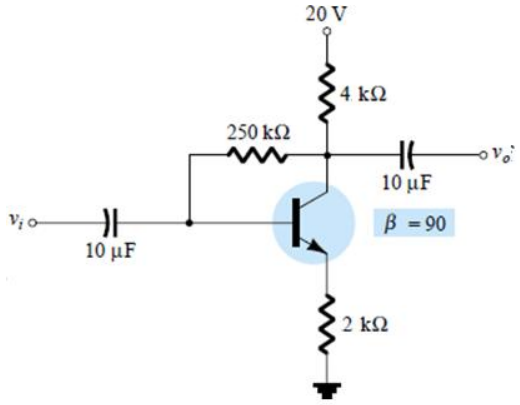
(The figures in the right hand margin indicate marks)

PART – A **(2 x 5 = 10 Marks)**

		CO #	Blooms Level
Q.1.	Answer ***ALL*** questions		
a.	A transistor has β of 100 and a base current, I_B, of 10 μ A. find the collector current, I_C.	CO1	K3
b.	Mention some of the linear applications of op – amps	CO2	K4
c.	Which gates are called as the universal gates? What are its advantages?	CO3	K3
d.	Reduce A'B'C' + A'BC' + A'BC	CO3	K3
e.	Differentiate between latches and flip-flop.	CO4	K4

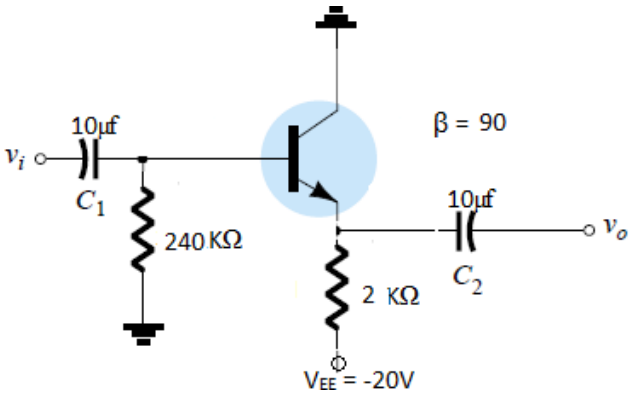
PART – B **(15 x 4 = 60 Marks)**

		Marks	CO #	Blooms Level
Answer ***ANY FIVE*** the questions				
2. a.		7	CO1	K3
	For the emitter bias network of Fig., determine			
b.	Determine the quiescent levels of I_{CQ} and V_{CEQ} for the network of Fig.	8	CO1	K3



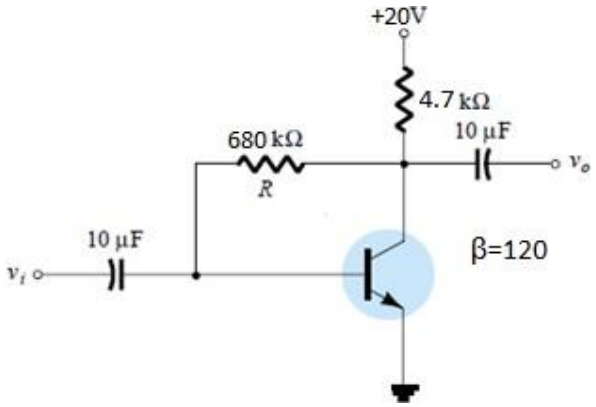
(OR)

c. Determine V_{CEQ} and I_E for the network of Fig.



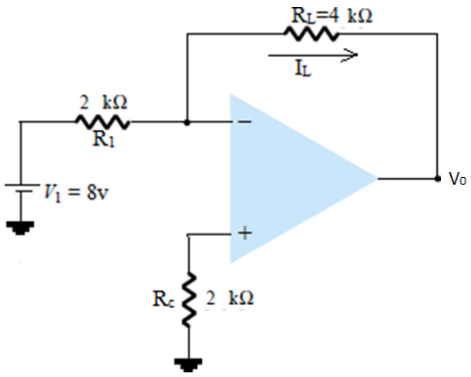
7 CO1 K3

d. For the network of Fig.
(i) Determine I_{CQ} and V_{CEQ}.
(ii) Find V_B, V_C, V_E, and V_{BC}



8 CO1 K3

3.a. For the circuit of Fig. calculate I_L & V_0

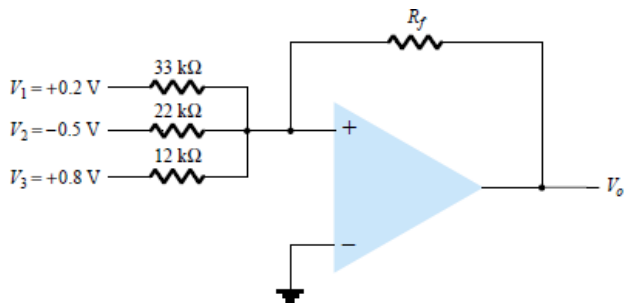


7 CO2 K3

b. Derive the formula for gain of inverting op-amp and find the output voltage for the circuit has R_1 = 100 kΩ and R_f = 500 kΩ, an input of V_1 = 2 V? 8 CO2 K4

(OR)

c. Calculate the output voltage developed by the circuit of Fig. for Rf =330 kΩ 7 CO2 K3



d. Design a 3 input Summing Amplifier using OP-Amp Write the equations with suitable diagram. 8 CO2 K4

4.a. Design the Full adder using NOR gates only. 7 CO3 K3

b. Design logic gate for Binary to BCD code Converter 8 CO3 K4

(OR)

c.	Express the Boolean function F = xy +x'z in a product of Maxterm form	7	CO3	K4
d.	Realize the following function of four variables with 8:1 MUX. $F(A,B,C,D) = \sum (0,1,3,5,7,11,13,15)$	8	CO3	K3
5.a.	Explain about Master Slave J-K flip-flop and its operation with suitable diagram.	7	CO4	K3
b.	Convert and draw the logic gate for the conversion of S-R to J-K Flip Flop	8	CO4	K4
	(OR)			
c.	Design a shift right SISO register using D Flip Flops. Show how a pulse 0101 is shifted using this type of register	7	CO4	K4
d.	Design a synchronous Mod-12 up counter.	8	CO4	K3

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