QP Code:RD22BTECH045 | Reg. No | | | | | | | | | | | AY 22

GIET UNIVERSITY, GUNUPUR – 765022

B. Tech (Third Semester Regular) Examinations, December – 2023

21BCSES23004 – Digital Electronics

(CSE, CSE(AIML), CSE(DS))

Time: 3 hrs | Maximum: 70 Marks

Answer all questions

(The figures in the right hand margin indicate marks)

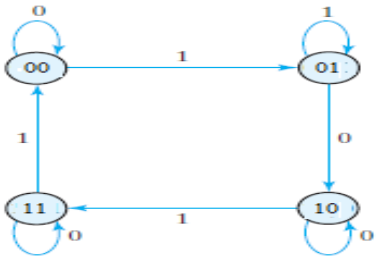
PART – A **(2 x 5 = 10 Marks)**

Q.1. Answer ***ALL*** questions	CO #	Blooms Level
a. Convert $(597)_{10}$ to BCD code.	CO1	K2
b. Show that the dual of the exclusive-OR is equal to its complement.	CO1	K1
c. Consider the function $f(x, y, z) = \sum(2, 3, 4, 6, 7)$. Derive the canonical sum of products for the function using minterm.	CO2	K2
d. What do you mean by sequential circuit? Hence distinguish between synchronous sequential circuits and asynchronous sequential circuits.	CO3	K2
e. How many 16K × 1 RAMs are required to obtain a memory with a word capacity of 64K? The word length is eight bits.	CO4	K3

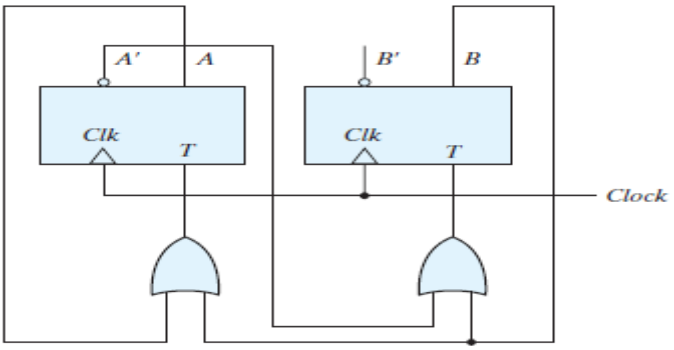
PART – B **(15 x 4 = 60 Marks)**

Answer ***ALL*** questions	Marks	CO #	Blooms Level
2. a. Construct logic circuit using AND, OR, and NOT gate for the following Boolean function: (i) $Y = (A + B)(A' + B')$ (ii) $Y = (A + B)(C' + D')(A' + C)$	8	CO2	K3
b. Subtract 101011_2 from 111001_2 using 1's complement and 2's complement methods.	7	CO1	K3
(OR)			
c. Apply DeMorgan's theorem to prove that $\overline{A\overline{B} + \overline{C}D + EF} = (\overline{A} + B)(C + \overline{D})(\overline{E} + \overline{F})$ Draw the corresponding logic circuit.	8	CO2	K3
d. Carry out the following additions: (i) (+13, -11) using 1's complement notation. (ii) (-15, +9) using 2's complement notation.	7	CO1	K3
3.a. Simplify the following Boolean function using K-map: $F(A, B, C, D) = \sum(4, 5, 6, 7, 12, 13, 14)$ and then, write the simplified function in SoP and PoS form.	10	CO2	K3
b. Implement the Boolean function $F(x, y, z) = \sum(1, 2, 6, 7)$ with a multiplexer.	5	CO2	K3
(OR)			
c. What is a full adder circuit? Draw its truth table. Design a full adder circuit using two half adder circuits and an 'OR' gate.	10	CO2	K3

d.	Implement the following Boolean function with a multiplexer. $F(A,B,C,D) = \sum(1,3,4,11,12,13,14,15)$	5	CO2	K3
4.a.	Draw the circuit diagram of a 2-bit by 2-bit binary multiplier using half-adders and logic gates. Explain its operation.	8	CO2	K3
b.	A *PN* flip-flop has four operations: no change, clear to '0', set '1', and complement; when inputs *P* and *N* are 00, 01, 10, and 11 respectively. Write the excitation table and characteristics equation of the *PN* flip-flop and realize the flip-flop using logic gates.	7	CO3	K3
	(OR)			
c.	A magnitude comparator is a combinational circuit that compares two numbers *A* and *B*, and determines their relative magnitudes. The outcome of the comparison is specified by three binary variables that indicate whether $A > B$, $A = B$ or $A < B$. Determine the algorithm to implement this comparator and draw a 2-bit magnitude comparator using the combinational circuit.	8	CO2	K3
d.	Describe the construction and operation of a master-slave flip-flop.	7	CO3	K3
5.a.	Design the sequential circuit specified by the state diagram of the figure using *JK* flip-flops.	10	CO3	K3



b.	Design a combinational circuit using a ROM that accepts 3-input and produces its 1's complement as output.	5	CO4	K3
	(OR)			
c.	Derive the state table and the state diagram of the sequential circuit shown in the figure.	10	CO3	K3



d.	Design a combinational circuit using a ROM. The circuit accepts a 3-bit binary number and generates an output binary number equal to the square of the input number.	5	CO4	K3

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