GIET UNIVERSITY, GUNUPUR – 765022

B. Tech (Third Semester - Regular) Examinations, December – 2022

21BCSES23001 / 21BCMES23001 / 21BCDES23001- DIGITAL ELECTRONICS

[CSE, CSE(AIML) and CSE(DS)]

Time: 3 Hours **Maximum: 70 Marks**

Answer *ALL* Questions.

(*The figures in the right-hand margin indicate marks.*)

PART – A (Short Answer Questions) **(2 × 5 = 10 Marks)**

Q.1. Answer ***ALL*** Questions.	CO #	Blooms Level
a. Convert 634_8 to binary, hexadecimal, and decimal.	CO1	2
b. State Distributive law of Boolean algebra.	CO1	1
c. Convert the following expression into a canonical sum of products: $Y = AC + AB + BC$.	CO2	2
d. Write a characteristic equation and excitation table for the *T* flip-flop.	CO3	1
e. Differentiate between static and dynamic RAM.	CO4	2

PART – B (Long Answer Questions) **(15 × 4 = 60 Marks)**

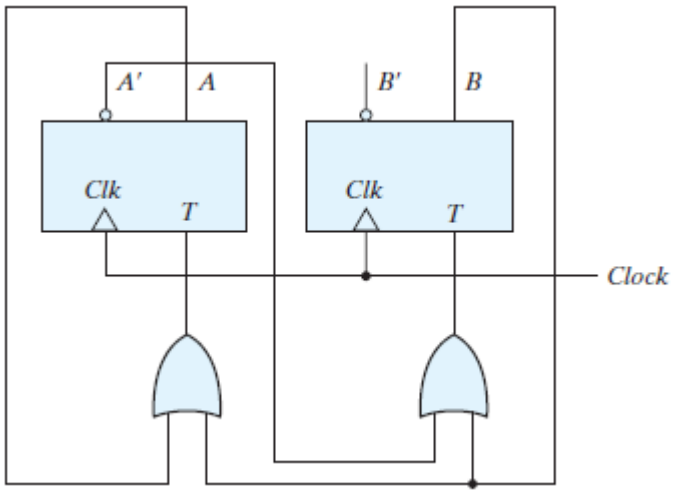
Answer ***ALL*** Questions.	Marks	CO #	Blooms Level
2. a. Carry out the following additions: (i) (+13, -11) using 1's complement notation. (ii) (-15, +9) using 2's complement notation.	8	CO1	3
b. Simplify the following Boolean functions to a minimum number of literals. (i) $x(x' + y)$ (ii) $xy + x'z + yz$	7	CO1	3
(OR)			
c. Apply DeMorgan's theorem to prove that $\overline{A\overline{B} + \overline{C}D + EF} = (\overline{A} + B)(C + \overline{D})(\overline{E} + \overline{F})$ Draw the corresponding logic circuit.	8	CO2	3
d. In a tabular form, write the "2421" code and "Excess-3" code of decimal digit "0 to 9". What are the special properties of these codes?	7	CO1	2
3. a. Simplify the following Boolean function using a four-variable K-map: $F(A, B, C, D) = \Sigma(0, 1, 3, 4, 5, 7, 9, 11, 15)$ and then, realize the simplified functions using logic gates.	8	CO2	3
b. Reduce the Boolean expression $A + B[AC + (B + \overline{C})D]$	7	CO1	3
(OR)			
c. What is a full adder circuit '? Draw its truth table. Design a full adder circuit using two half adder circuits and an 'OR' gate.	8	CO2	3
d. Implement the Boolean function $F(A, B, C, D) = \sum(1, 3, 4, 11, 12, 13, 14, 15)$ with a multiplexer.	7	CO2	3
4. a. Draw the circuit diagram of a 2-bit by 2-bit binary multiplier using half-adders and logic gates. Explain its operation.	8	CO2	3
b. Construct a 4-to-16-line decoder with two 3-to-8-line decoders with enable.	7	CO2	3

(OR)

c.	Write short notes on Master slave *JK* flip-flop.	8	CO3	2
d.	Explain how a *J-K* can be constructed using *D* flip-flop.	7	CO3	3
5. a.	Design a counter with the following repeated binary sequence: 0, 1, 2, 4, 6. Use *D* flip-flops.	8	CO3	3
b.	What is a shift register? Explain the principle of a 4-bit serial-in, parallel-out, shift register.	7	CO3	2

(OR)

c.	Derive the state table and the state diagram of the sequential circuit shown in the figure.	8	CO3	3



d.	How many 32K × 8 RAM chips are needed to provide a memory capacity of 256K bytes? How many lines of the address must be used to access 256K bytes? How many of these lines are connected to the address inputs of all chips? How many address lines must be decoded for the chip select input? Specify the size of the decoder.	7	CO4	3

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