QPC: RJ19BTECH131 AR 19 Reg. No | | | | | | | | | | |

GIET UNIVERSITY, GUNUPUR – 765022

B. Tech (Fourth Semester – Regular) Examinations, June – 2021

BPCCS4020 / BPCCT4020 - Computer Organization and Architecture

(CSE & CST)

Time: 2 hrs Maximum: 50 Marks

Answer ALL Questions

The figures in the right hand margin indicate marks.

PART – A: (Multiple Choice Questions) (1 x 10 = 10 Marks)

Q.1. Answer ***ALL*** questions [CO#] [PO#]

a. For comparing the performance of a new system, the users will simply compare execution time of its — 2 1

(i) Response Time (ii) Workloads

(iii) Execution Time (iv) Multitasking

b. In CISC architecture most of the complex instructions are stored in — 1 1

(i) Register (ii) Diodes

(iii) CMOS (iv) Transistors

c. A multiprocessor operating system should perform — 2 1

(i) a mechanism to split a task into concurrent subtasks (ii) optimise the system performance

(iii) handling structural or architectural changes (iv) all of the mentioned

d. If the control signals are generated by combinational logic, then they are generated by a type of _____ controlled unit — 2 1

(i) Micro programmed (ii) Software

(iii) Logic (iv) Hardwired

e. MIMD stands for — 4 1

(i) Multiple instruction multiple data (ii) Multiple instruction memory data

(iii) Memory instruction multiple data (iv) Multiple information memory data

f. Floating point representation is used to store — 3 1

(i) Boolean values (ii) Whole numbers

(iii) Real integers (iv) Integers

g. The result obtained on binary multiplication of 1010 * 1100 is — 3 3

(i) 0001111 (ii) 0011111

(iii) 1111100 (iv) 1111000

h. Write Through technique is used in which memory for updating the data — 4 1

(i) Virtual memory (ii) Main memory

(iii) Auxiliary memory (iv) Cache memory

i. The LRU provides very bad performance when it comes to _____ — 4 1

(i) Blocks being accessed is sequential (ii) When the blocks are randomised

(iii) When the consecutive blocks accessed are in the extremes (iv) None of the mentioned

j. In a data transfer operation involving SCSI BUS, the control is with — 4 1

(i) Initiator (ii) Target

(iii) SCSI controller (iv) Target Controller

PART – B: (Short Answer Questions) **(2 x 5 = 10 Marks)**

Q.2. Answer ***ALL*** questions		[CO#]	[PO#]
a.	What is an instruction set architecture in computer science?	1	1
b.	What happens when branch instruction comes in the program?	1	1
c.	What are the advantages of array processor?	2	2
d.	What rules are used in binary division?	3	1
e.	Why interfacing is needed for I/O devices?	4	1

PART – C: (Long Answer Questions) **(6 x 5 = 30 Marks)**

Answer ***ANY FIVE*** questions		Marks	[CO#]	[PO#]
3.	Explain the functional units of a digital computer with the help of its block diagram.	(6)	1	1
4.	What are the advantages of high level language over machine language?	(6)	1	1
5.	What are the principles of linear pipelining and how these pipeline processors can be classified?	(6)	2	1
6.	Explain the Flynn's computer classification schemes with the help of suitable diagrams.	(6)	2	1
7.	Define full adder and explain its working with the help of circuit diagram.	(6)	3	1
8.	Explain about the representation of floating point numbers with suitable examples.	(6)	3	1
9.	Explain the following with the help of example: (i) Direct mapping (ii) Associative mapping	(6)	4	1
10.	What do you mean by Page Fault? Discuss any two page replacement algorithms.	(6)	4	1

--- END OF PAPER ---