DE (BPCEC4010) Key for SET-1 (2021)

Section – A 10 Questions (2 Marks each) total 20 Marks		
Q1	**MCQ**	
A	ii	
B	i	
C	i	
D	iii	
E	i	
F	iv	
G	iv	
H	iii	
I	iii	
J	iii	
Section – B 10 Questions (2 Marks each) total 20 Marks		
Q2	**SAQ**	
A	Procedure 1 Mark and example 1Mark	
B	Finding –y, 1Mark and correct answer 1 Mark	
C	Statement ½ Mark Formula ½ Mark Example 1 Mark	Associative law. A binary operator * on a set S is said to be associative whenever $(x * y) * z = x * (y * z)$ for all $x, y, z \in S$
D	Logic definition 1 Mark and simple circuit/block diagram 1 Mark	
E	Proper explanation 2 Mark	
F	Definition 1 Mark Explanation 1 Mark	
G	Basic logic definition 1 Mark and explanation 1 Mark	
H	Mod -5 definition 1Mark and explanation 1 Mark	
I	Proper explanation 2 Mark.	
J	Proper explanation 2 Mark.	
Section – C 4 Questions (15 Marks each) total 60 Marks		
Q3	**LAQ**	

a Any five

1)

1. The structure is closed with respect to the operator + .
2. The structure is closed with respect to the operator $\cdot$.

2)

1. The element 0 is an identity element with respect to + ; that is, $x + 0 = 0 + x = x$.
2. The element 1 is an identity element with respect to $\cdot$; that is, $x \cdot 1 = 1 \cdot x = x$.

3)

1. The structure is commutative with respect to + ; that is, $x + y = y + x$.
2. The structure is commutative with respect to $\cdot$; that is, $x \cdot y = y \cdot x$.

4)

1. The operator $\cdot$ is distributive over + ; that is, $x \cdot (y + z) = (x \cdot y) + (x \cdot z)$.
2. The operator + is distributive over $\cdot$; that is, $x + (y \cdot z) = (x + y) \cdot (x + z)$.

5) For every element x ∈ B , there exists an element x′ ∈ B (called the complement of x) such that (a) x + x′ = 1 and (b) x · x′ = 0.
6) There exist at least two elements x , y ∈ B such that x ≠ y .
Comparing Boolean algebra with arithmetic and ordinary algebra **5 Marks**

b

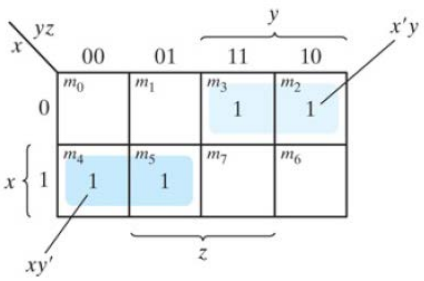
Finding F2 (F2= x'y'z + x'yz' + x'y) **3.5 Marks** and finding x, y and z(for ex. x=0, y=0 and z=1) **1.5 Marks**

.OR

c Implementation using given logic gates **3 Marks**

d Correct K-Map **3 Marks** , Function deriving **2 Marks,** function implementation **1 Mark** and function testing **1 Mark**

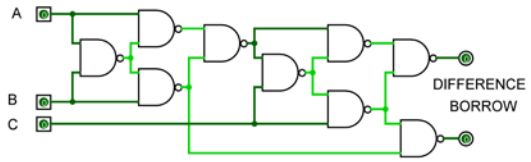
F=x'y+xy'



Q4 LAQ

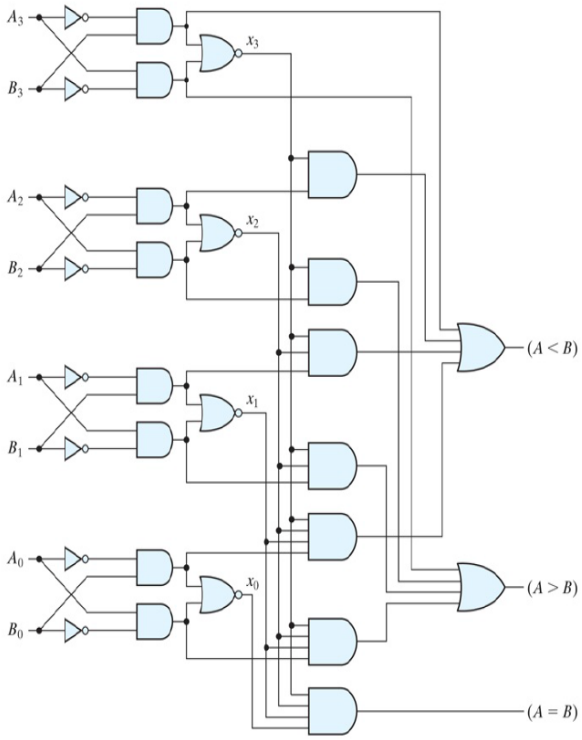
a Decoder circuit/block diagram **3 Marks** and explanation **2 Marks**

b Circuit **3 Marks** and testing **2 Marks**



OR

c The design will get **3 Marks** and explanation design will get **2 Marks**

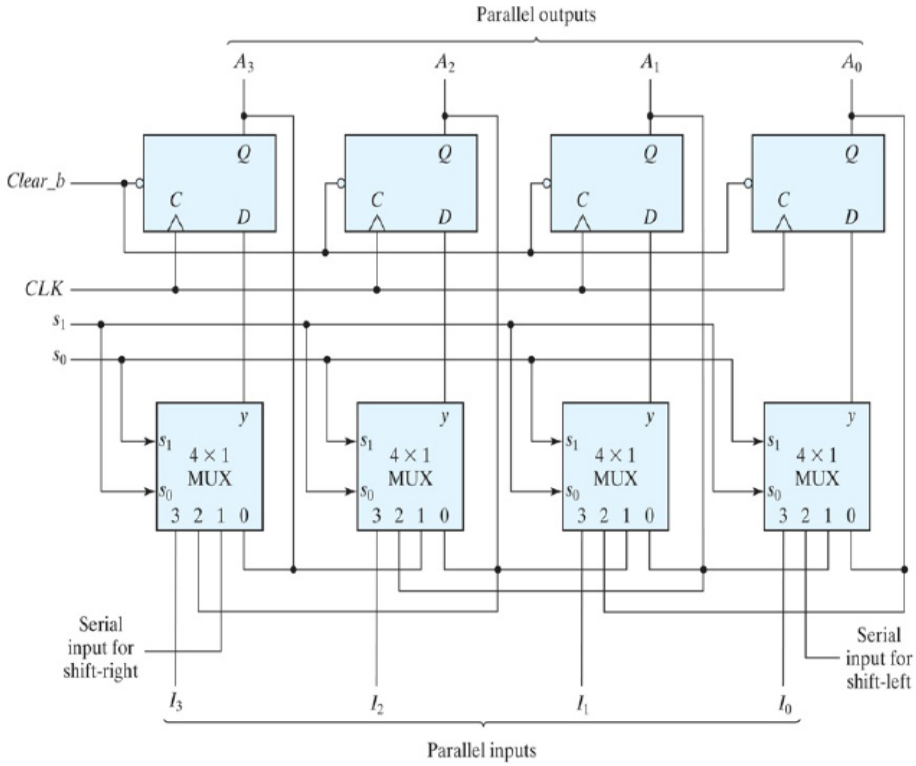


d

The design will get **3** **Marks** and explanation design will get **2** **Marks**

Q5 **LAQ**

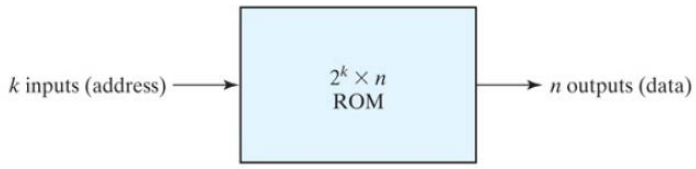
a Circuit diagram **5** **Marks** and explanation **3** **Marks**



b Proper explanation **2** **Marks**

OR

c ROM design **3** **Marks** and explanation **3** **Marks**

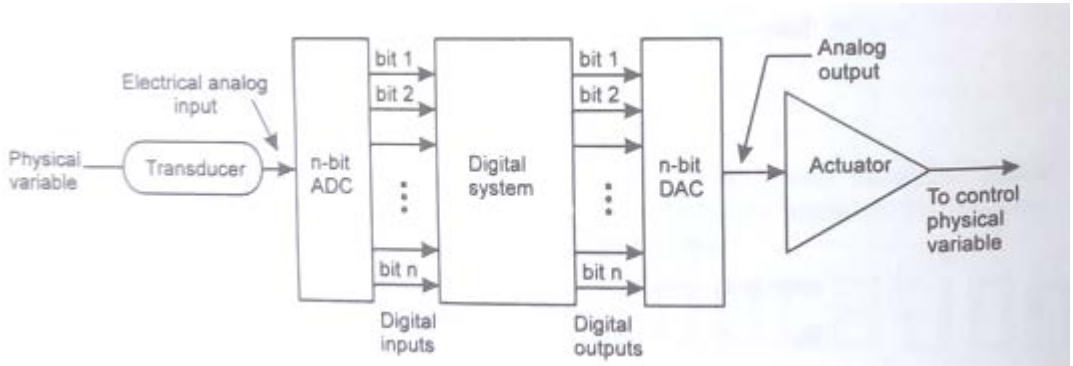


d

Different types of RAMs like Dynamic, Static explanation **4** **Marks**

Q6 **LAQ**

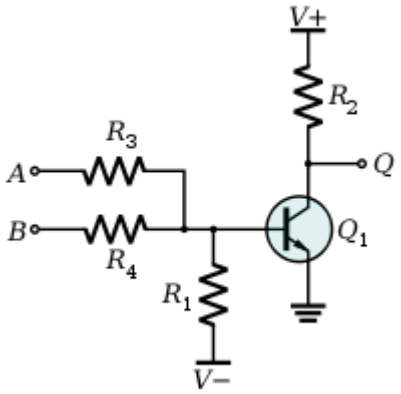
a Proper assumption (below diag.) **4** **Marks** and explanation **4** **Marks**



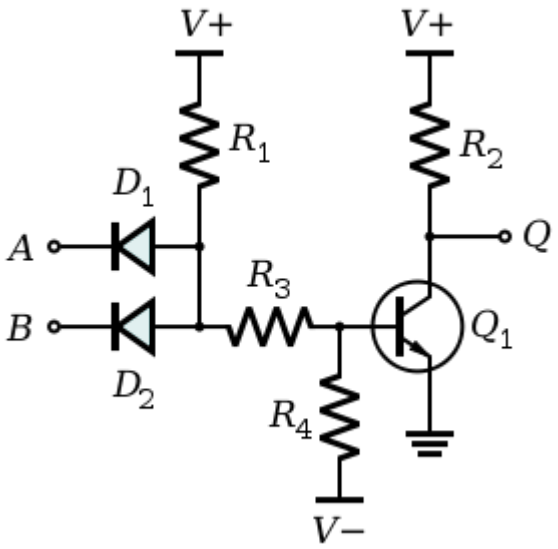
b Proper explanation **2** **Marks**

OR

c Circuit **3** **Marks** and explanation **2** **Marks**



d Circuit **3** **Marks** and explanation **2** **Marks**



(Basic 2 input NAND using DTL)