QP Code:RD18001035 Reg. No | | | | | | | | | | | AR 18

GIET MAIN CAMPUS AUTONOMOUS GUNUPUR – 765022

B. Tech Degree Examinations, December – 2020

(Fifth Semester)

BECPC 5030 / BEIPC 5030 – DIGITAL VLSI DESIGN

(AEI & ECE)

Time: 2 hrs Maximum: 50 Marks

The figures in the right hand margin indicate marks.

PART – A: (Multiple Choice Questions) (1 × 10=10 Marks)

Q.1. Answer ***ALL*** questions [CO#] [PO#]

a. MOSFET has greatest application in digital circuit due to_____ CO1 PO1
(i) Low power consumption (ii) Less noise
(iii) Small amount of space it takes on a chip (iv) All of the above

b. The width of n-diffusion and p-diffusion layer should be ____ [CO1] [PO2]
(i) 3λ (ii) λ
(iii) 2λ (iv) 4λ

c. In inverter circuit _____ transistors is used as load. CO2 PO1
(i) Enhancement mode (ii) Depletion mode
(iii) All of the mentioned (iv) None of the mentioned

d. For better noise immunity, the NM for low signal should be at least _____percentage of $V_{DD.}$ CO2 PO2
(i) 25 (ii) 10
(iii) 50 (iv) 75

e. The output of sequential circuit is regarded as a function of time sequence of _____. CO3 PO1
(i)) Inputs & Outputs (ii) Outputs & Internal states
(iii) Inputs & Internal states (iv) External states

f. AND operations are performed by _____connected drivers in pull-down network. CO3 PO3
(i) Series (ii) Parallel
(iii) Parallel-series (iv) Series-parallel

g. To design transistor-level schematic of the one-bit full-adder circuit _____ total number of pMOS transistors required. CO3 PO3
(i) 12 (ii) 28
(iii) 14 (iv) 10

h. Voltage bootstrapping is used for_____. CO4 PO1
(i) Overcoming threshold voltage drops (ii) Constant threshold voltage drops
(iii) Overcoming sub-threshold voltage (iv) Overcoming sub-threshold current

i. When the clock signal becomes high in dynamic logic, the circuit is operating in_____. CO4 PO2
(i) Evaluate phase (ii) Static phase
(iii) Precharge phase (iv) Dynamic phase

j. The most significant disadvantage of using a pseudo-nMOS gate instead of a full-CMOS gate is _____ static power dissipation. CO3 PO2
(i) Zero (ii) Nonzero
(iii) None of the mentioned (iv) No

PART – B: (Short Answer Questions) **(2 × 5 = 10 Marks)**

Q.2. Answer ***ALL*** questions	[CO#]	[PO#]
a. Why positive photoresist is preferred over negative photoresist?	[CO1]	[PO1]
b. Write down the advantages of CMOS inverter.	CO2	PO1
c. Show how interconnect delay dominates gate delay in submicron CMOS technologies.	CO2	PO1
d. Design the stick diagram of XNOR logic gate.	CO3	PO3
e. Define two-phase clocking scheme.	CO4	PO3

PART – C: (Long Answer Questions) **(6 × 5 = 30 Marks)**

Answer ***ANY FIVE*** questions	Marks	[CO#]	[PO#]
3. Explain the VLSI design flow in Y-chart.	6	CO1	PO1
4. Derive the linear and saturation drain current in Gradual Channel Approximation of nMOS transistor.	6	CO1	PO2
5. Explain the CMOS inverter circuit with VTC and derive the expressions for all the critical voltages with NM calculation.	6	CO2	PO2
6. Differentiate propagation delay, rise time and fall time with proper diagram of CMOS inverter.	6	CO2	PO1
7. Find an equivalent CMOS inverter circuit of the logic function Z= {(A+B+C)(D+E)}' by assuming that $(W/L)_p$ = 12 for all pMOS transistors and $(W/L)_n$ = 8 for all nMOS transistors.	6	CO3	PO3
8. Explain the design of NOR-based realization of the JK master-slave flip-flop.	6	CO3	PO3
9. Explain Dynamic bootstrapping with proper diagram.	6	CO4	PO3
10 Design the Boolean function, Z = PQ + (R + S) TU + VW by using standard CMOS and domino CMOS.	6	CO4	PO3

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