Registration No. : | | | | | | | | | | |

Total number of printed pages – 2

B. Tech

PCEC 4401C

Seventh Semester Examination – 2011

VLSI DESIGN

Full Marks – 70

Time : 3 - Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*
The figures in the right-hand margin indicate marks.
Assume any data if not given i the question.

1. Answer the following questions : 2×10

   (a) What is the difference of VLSI design and VLSI technology ?

   (b) Mention the hierarchy of classification of CMOS digital circuits.

   (c) Draw the input and output characteristics of depletion type MOSFET.

   (d) What is flat band voltage and how is it related to surface potential of MOSFET ?

   (e) What is surface inversion? Draw its energy band diagram ?

   (f) How substrate bias effect is affecting to the threshold voltage of MOSFET ?

   (g) What is the need of scaling in VLSI ?

   (h) Implement two input XOR gate using transmission gate or pass transistor gate.

   (i) What is LOCOS ?

   (j) Explain in brief the various power dissipations in CMOS inverter.

2. (a) Draw and explain the fabrication process steps of CMOS n-well process. 5

   (b) Discuss the standard VLSI design methodology. 5

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3. (a) What is threshold voltage of MOSFET ? Derive its expression for both n-channel and p-channel MOSFET. 5

(b) Discuss the operation of MOSFET by drawing its energy band diagrams in all modes of operation. 5

4. (a) Discuss the Latch up problem in CMOS circuits. How can it be avoided ?

(b) Discuss the operation of CMOS inverter by drawing the VTC and derive the expression of critical voltages. 5

5. (a) Implement the following Boolean expression $Z = \overline{A(B + C)D}$ using dynamic CMOS logic. Draw the timing diagram of precharge and evaluation cycle. Explain the cascading problem in dynamic CMOS logic and how does it overcome ? 5

(b) Implement the above Boolean function using Domino CMOS logic and pseudo nMOS logic. 5

6. (a) Differentiate between τ_{PHL} and τ_{PLH}. Derive the expression of τ_{PLH}. How do you calculate the average propagation delay ? 5

(b) How do you calculate the interconnect delay using RC Delay models and the Elmore Delay model ? 5

7. (a) Explain the basic principle of Pass transistor circuits mentioning Logic '1' transfer and Logic '0' transfer. 5

(b) Discuss the various configurations of the dynamic RAM cell. Explain the operation of 1 bit DRAM cell. 5

8. Write short notes on any *two* : 5×2

(a) Standard Cell based Design

(b) MOSFET Model

(c) CMOS Technology