Registration No. : | | | | | | | | | | |

Total number of printed pages – 3

B. Tech

PCEC 4401A

Seventh Semester Examination – 2011

VLSI DESIGN

Full Marks – 70

Time : 3 - Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*

The figures in the right-hand margin indicate marks.

Assume any data if not given in the question.

1. Answer the following questions : 2×10

(a) What is the difference between full-custom and semi-custom design ?

(b) Draw the Gajski Y-chart for HDL based design.

(c) What is FPGA ?

(d) What is channel length modulation ?

(e) What is the condition of strong inversion in MOSFET, explain in brief using energy band diagram ?

(f) What do you mean by substrate bias effect ?

(g) What are the MOS SPICE parameters ?

(h) What is the difference between enhancement and depletion type MOSFET ?

(i) What is noise margin and noise immunity? How are they related ?

(j) Draw the circuit of 1bit DRAM memory cell.

2. (a) Explain the VLSI design flow using suitable diagram. 4

(b) What are the measures of design qualities of IC Design ? 3

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(c) Explain how CAD tools are useful in VLSI Design. Name few of the tools and write its usage. 3

3. (a) What is the need of Scaling in IC Design ? What are its advantages and disadvantages ? Discus the types of Scaling. 4

(b) What are the short channel effects in MOSFET ? 3

(c) Draw the Fabrication process steps of n-MOSFET using proper color coding. 3

4. (a) Derive the drain current equation of MOSFET in all modes of operation and draw the V~I characteristics with and without channel length modulation. 4

(b) Draw the energy band diagram of three different operating modes of MOS system under external bias and derive the expression of maximum depletion width. 3

(c) Discuss the C~V characteristics of MOSFET during low frequency and high frequency operation. 3

5. (a) Discuss the operation of CMOS inverter by drawing its Voltage Transfer Characteristics (VTC) and show the various critical voltages in different regions of the VTC. 4

(b) Derive the expression of switching threshold voltage. 3

(c) Discuss the supply voltage scaling, power and area considerations in CMOS inverters. 3

6. (a) Consider a resistive-load inverter circuit with $V_{DD}=5V$, $k_n'=10\mu A/V^2$, $V_{T0}=0.8V$, $R_L=100k\Omega$ and $W/L=2$. Calculate the critical voltages on the Voltage Transfer Characteristics (VTC) and find the noise margins of the circuit. 4

(b) Show that for an ideal symmetric CMOS inverter the $(W/L)_p$ is 2.5 times the $(W/L)_n$. 3

(c) What are the various leakage currents in CMOS inverter ? 3

7. (a) Discuss the switching characteristics of CMOS inverter and derive the expressions of τ_{PHL}. 4

(b) What is sheet resistance and what is its use in VLSI ? 3

(c) What are the delay models exist for the estimation of interconnect delay ? Explain any one of the model. 3

8. (a) Implement the Boolean function $Z = \overline{A(B+C)+D}$ using pseudo nMOS logic. Find an equivalent CMOS inverter circuit for simultaneous switching of all inputs, assuming that $(W/L)_p$=10 for all p-MOS transistors and $(W/L)_n$= 5 for all n-MOS transistors. 4

(b) Implement the two input XOR gate using pass transistor logic and transmission gate. 3

(c) Implement the D-latch circuit using CMOS and draw its timing diagram showing setup time and hold time. 3
