Registration No. : | | | | | | | | | | |

Total number of printed pages – 3

B. Tech

FECE 6401

Seventh Semester Examination – 2011

COMPUTER SYSTEM ARCHITECTURE

Full Marks – 70

Time : 3 - Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*

The figures in the right-hand margin indicate marks.

1. Answer the following questions : 2×10

(a) What do you mean by word aligned address ?

(b) What is the difference between Little-endian and Big-endian formats ?

(c) What do you mean by associativity of a cache mapping technique ? What is the associativity of direct mapping technique ?

(d) With a suitable example define indexed addressing mode.

(e) Represent binary number 1101.00101 in IEEE 754 32 bit single precision standard.

(f) What is the difference between Horizontal and Vertical organization of Microinstruction ?

(g) What is memory interleaving ? How block transfer time reduces using interleaving technique ?

(h) What are the different types of misses in cache ? What do you mean by miss penalty ?

(i) What do you mean by push-down stack ? What is the behavior of SP in push down stack ?

P.T.O.

(j) What is the use of ORG and EQU directives in assembly language programming ?

2. (a) With neat circuit diagram discuss the algorithm for restoring division. 5

(b) Perform the following division using non-restoring method : 5

$A = 10101 \quad B = 00101, \quad A \div B = ?$

3. (a) Design 16 bit carry-lookahead adder from 4bit adders by using higher level block generate and propagate function and calculate the gate delay to generate C_{16} and S_{15}. Compare these delays with ripple carry method for 16 bit. 5

(b) What is Bit-Pair Recording method for fast multiplication ? With Suitable example discuss how it works. Multiply these two signed 2'complement numbers using booth's algorithm. A = 110101 B = 001111.

4. (a) Draw a neat diagram and discuss three bus organization of the data-path. Write the control sequence required to Fetch and Execute ADD Instruction on the same. 5

(b) With schematic diagram discuss the Micro-program control unit. Compare the performance of micro-programmed control and hardwired control. 5

5. (a) How page translation is performed in virtual memory organization ? How using TLB the address translations can be performed faster ? Discuss with suitable diagram. 5

(b) For a virtual memory organization having 80 GBytes of Virtual Memory and 1 GBytes of Physical Memory and a page size of 4 KBytes. Find out the number of entries in the page table, Also find out the size of page frame field in the page table. 5

6. (a) What is the role of mapping function in cache organization ? Discuss the Direct Mapping technique in detail. Also discuss different cache writing algorithms. 5

(b) A block set associative cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 block, each consisting of

128 words of 32bit each. Calculate how many bits are there in a main memory address ? Also calculate how many bits are there in each of the TAG, SET and WORD Fields ? 5

7. (a) What is the job of MMU in the memory system ? What are the difference page replacement policies ? Discuss them in detail. 5

(b) In a memory hierarchy having L1 and L2 cache with a hit rate of 0.9 and 0.85 respectively and access time on 3 nsec and 11 nsec respectively. If Average access time of main memory is 150 nsec then what is the average time of the memory system ? 5

8. Write short notes on any *two* : 5×2

(a) SDRAM

(b) RAID Disk Array

(c) RISC Vs CISC.