Registration No. : | | | | | | | | | | |

Total number of printed pages – 3

B. Tech

PCEC 4401

Seventh Semester Examination – 2013

VLSI DESIGN

BRANCH : EC, IEE, AEIE, ETC

QUESTION CODE : C-291

Full Marks – 70

Time : 3 Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*

The figures in the right-hand margin indicate marks.

1. Answer the following questions : 2×10

   (a) What do you mean by threshold voltage of MOSFET ? Write down the expression for threshold voltage of a NMOS and PMOS.

   (b) Design the function $F = \overline{(A \cdot B + C)}$ using CMOS logic and find out the equivalent (W/L) ratios considering symmetrical MOSFETS.

   (c) Realize a 2-input XOR gate using CMOS transmission gate.

   (d) What is surface inversion ? Draw its energy band diagram.

   (e) Draw the circuit of 1-bit DRAM cell.

   (f) What is I_{DDQ} testing ?

   (g) Design the pull up network of a 2-input CMOS XOR gate.

   (h) How many devices can be fabricated on a 4 inch Silicon wafer by using 2 μm technology ?

   (i) A logic gate has $V_{OH} = 5V$, $V_{OL} = 0.2V$, $V_{IH} = 0.5V$ and $V_{IL} = 0.8V$. Calculate the noise margins.

   (j) Draw the stick diagram of a two input CMOS NAND gate.

P.T.O.

2. (a) Derive and calculate the switching threshold voltage V_{th} of the two input CMOS NOR gate with the following parameters : 5

$(W/L)_p = 4$, $(W/L)_n = 1$, $V_{T0n} = |V_{T0p}| = 0.7V$, $\mu_n C_{ox} = 40\mu A/V^2$, $\mu_p C_{ox} = 20\mu A/V^2$ and $V_{DD} = 5V$.

(b) Derive the current equation using the gradual channel approximation theory for a p-channel MOS transistor operating in the linear region, i.e, for $V_{SG} + V_{TP} > V_{SD}$. 5

3. (a) Calculate the values of V_{OH}, V_{OL}, V_{IL}, V_{IH} and noise margins for a saturated enhancement type load NMOS inverter circuit. Given $V_{DD} = 5V$, $V_T = V_{T0} = 0.8V$ and $(K_{driver}/K_{load}) = 10$. 5

(b) Design a circuit described by the function $Y = \overline{\{A \cdot (B+C) \cdot (D+E)\}}$ using CMOS logic. Also find the equivalent CMOS inverter circuit for simultaneous switching of all inputs assuming that $(W/L)_p = 5$ for all PMOS transistors and $(W/L)_n = 2$ for all NMOS transistors. 5

4. Measured voltage and current data for a MOSFET is given below : 10

V_{GS} (V)	V_{DS} (V)	V_{SB} (V)	I_D (μA)
3	3	0	97
4	4	0	235
5	5	0	433
3	3	3	59
4	4	3	173
5	5	3	347

Determine the type of device, mode of operation and calculate the parameters k, V_{T0} and γ. Given $\phi_F = -0.3V$.

5. (a) Implement the following Boolean expression $Z = \overline{\{A \cdot (B+C) \cdot D\}}$ using dynamic CMOS logic. Draw the timing diagram of precharge and evaluation cycle. Explain the cascading problem in dynamic CMOS logic and how does it overcome ? 5

(b) Implement the above Boolean function using Domino CMOS logic and Pseudo NMOS logic. 5

6. (a) Draw the energy band diagram of three different operating modes of MOS system under external bias and derive the expression of maximum depletion width. 5

(b) Draw the circuit diagram and corresponding stick diagram of a 3 input NAND gate using CMOS technology. 5

7. (a) Calculate the change in the noise margin of a resistive load inverter, if load resistance changes from 200 kΩ to 300 kΩ . The process parameter for driver transistor are $K_n = 50\,\mu A/V^2$, $V_{T0} = 1$ V and $V_{DD} = 5$ V. 5

(b) Derive an expression for the high to low propagation delay (τ_{PHL}) of a CMOS Inverter. 5

8. Write short notes on any **two** : 5×2

(a) Flash memory

(b) FPGA

(c) Current monitoring I_{DDQ} testing

(d) MOS Capacitances.