Regi	istrat	tion No. :		
Total number of printed pages – 2 B. Tech				
			FECE 6401	
		Seventh Semester Examination – 2013		
		COMPUTER SYSTEM ARCHITECTURE		
		BRANCH: IEE, ETC, EC, AEIE		
		QUESTION CODE: C-167		
Full Marks - 70				
		Time: 3 Hours		
. A	nswe	er Question No. 1 which is compulsory and any five from t The figures in the right-hand margin indicate marks.	he rest.	
1.	Write	e short notes on the following:	2×10	
(A)	(a)	Big-endian representation		
	(b)	Subroutine		
	(c)	Memory-mapped I/O		
	(d)	Emulation		
	(e)	Microinstruction		
	(f)	Virtual Memory		
	(g)	Paging		
	(h)	Program Controlled I/O		
	(i)	CISC		
	(j)	Secondary Storage.		
2	(a)	With a suitable diagram discuss the basic function avaits of a (	Computer.	

Write the truth table and design the logic circuit of a full-adder.

(b) With a suitable diagram explain inst

sequencing.

3.

(a)

P.T.O.

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	(b)	What are carry generate (G <sub>i</sub> ) and carry propagate (P <sub>i</sub> ) functions. Explain	
		the carry of each stages of a 4-stage adder. 5	
4.		What do you understand by addressing modes? Discuss with suitable	
		examples five different addressing modes that you know. 10	
5.	(a)	Design and explain the circuit arrangement of binary division 5	
	(b)	Explain a 4-bit example as it would be processed by the circuit in (a) above.	
6.	(a)	Discuss the double precision IEEE standard floating-point format to represent decimal 123.5.	
	(b)	Write the Add/ Subtract, Multiply and Divide rules on floating-point	
		numbers. 5	
7.	(a)	Explain the execution of the complete instruction ADD (R3),R1. 5	
	(b)	With a suitable block diagram discuss hardwired control unit, separating	
		the decoding and encoding functions. 5	
8.	Ans	ver the following questions: 2.5×4	
	(a)	Discuss direct-mapped cache with a suitable diagram.	
	(b)	With a suitable diagram explain set-associative mapped cache with two	
		Bepresentation of negative numbers	
	(c)	Representation of negative numbers	
	(d)	Memory Management requirements.	