Registration No. : | | | | | | | | | | |

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B. Tech

PCEC 4401

Seventh Semester (Special) Examination – 2013

VLSI DESIGN

BRANCH : CSE, EEE, ELECTRICAL, IT

QUESTION CODE : D 458

Full Marks – 70

Time : 3 Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*

The figures in the right-hand margin indicate marks.

1. Answer the following questions:

   (a) Define the terms Regularity, Modularity and Locality.

   (b) Why is Silicon preferred over other semiconductor materials in the IC Industry ?

   (c) What is the difference between full custom and FPGA design styles ?

   (d) Draw the stick diagram and the layout diagram of a 2-input NAND gate.

   (e) Calculate the oxide capacitance for a MOS capacitor for the oxide thickness, $t_{ox} = 100\text{Å}$. Assume $\varepsilon_{ox} = 3.97\,\varepsilon_o$

   (f) Draw the CMOS implementation of a NOT gate. What is the minimum power supply voltage required for a CMOS inverter so that it can operate properly.

   (g) Implement a 2 input XOR gate using transmission gates.

   (h) If a domino gate input is initially a '1' at the start of evaluation, can it make any other transition during evaluation? Why or Why not ?

   (i) Implement an edge triggered DFF using CMOS.

   (j) What is CPL logic ? Give one advantage of this style of implementation.

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2. (a) Calculate the threshold voltage of a NMOS transistor with substrate grounded and the following parameters-Substrate and the polysilicon gate doping are respectively given as $N_{A(substrate)} = 1.5 \times 10^{15}/cm^3$, $N_{D(PolySi\ gate)} = 1 \times 10^{20}/cm^3$. The oxide thickness is t_{ox}=1000Å and the fixed oxide charge, $Q_{OX} = q.1 \times 10^{10} C/cm^2$. Assume no threshold adjust implantation impurities are added. 5

(b) Draw and explain the Y-Chart for VLSI Design Flow. 5

3. (a) For the nMOS enhancement mode transistor, calculate the drain current for $\lambda = 0.05V^{-1}$ and $\left(\frac{W}{L}\right) = 2$. Given that $K'_n = \mu_n C_{ox} = 20\ \mu A/V^2$, $\left(\frac{L}{L_{eff}}\right) = \frac{1}{2}$, VG = 3V, VS = 1V, VD = 5 V, VT0 = 1 V. What does this result indicate ? 5

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(b) Derive the current equation using the gradual channel approximation theory for a n–channel MOS transistor operating in the linear region. 5

4. Design a transistor-level CMOS logic circuit to implement a 2×1 MUX using the following styles: Static CMOS, Dynamic CMOS, Pseudo NMOS and Domino Logic. 10

5. (a) With the help necessary band diagram show the electrical behaviour of a MOS system at "surface inversion". Derive the maximum depletion depth during this condition. 5

(b) Explain the VTC of a CMOS Inverter with proper labeling. Also derive the V_{OH} and V_{oL} of a CMOS Inverter. 5

6. (a) Define the terms rise time and fall time with suitable diagrams. How does the C_{load} effect propagation delay of a circuit ? 5

(b) What are the precharge and evaluate phase of a dynamic logic ? Name two techniques to avoid the problem of charge sharing in dynamic circuits. Give suitable diagrams to aid yours answer. 5

7. (a) Design a circuit described by the function $Y = \overline{A \cdot (B + C) \cdot (D + E)}$ using CMOS logic. Also find the equivalent CMOS inverter circuit for simultaneous switching of all inputs assuming that $\left(\frac{W}{L}\right)_p = 5$ for all ***p***MOS transistors and $\left(\frac{W}{L}\right)_n = 2$ for all ***n***MOS transistors. 5

(b) Calculate the switching threshold voltage V_{th} of the two-input CMOS NOR gate with the following parameters : $(W/L)_p = 4$, $(W/L)_n = 1$, $V_{Ton} = 0.7V$, $V_{Top} = -0.7V$, $\mu_n C_{ox} = 40\ \mu A/V^2$, $\mu_p C_{ox} = 20\ \mu A/V^2$, $V_{DD} = 5V$. Compare the result with the switching threshold voltage V_{th} of a CMOS inverter with the same parameters. 5

8. Write short notes on any **two** of the following : 5×2

(a) PMOS Fabrication Steps

(b) MOSFET Capacitance

(c) Small Geometry effects

(d) 1T DRAM Cell

(e) BIST.

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