Registration No. : | | | | | | | | | | |

Total number of printed pages – 3

B. Tech

CPEC 5403

Seventh Semester (Special) Examination – 2013

VLSI DESIGN

BRANCH CODE : AEIE, EC, ETC, IEE

QUESTION CODE : 469

Full Marks – 70

Time : 3 Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*
The figures in the right-hand margin indicate marks.

1. Answer the following questions : 2×10

   (a) State the four different types of CMOS process you are familiar with.

   (b) With a suitable diagram show the different layers in a MOS transistor.

   (c) What is stick diagram and what are the uses of stick diagram ?

   (d) Define threshold voltage in CMOS.

   (e) What is channel-length modulation ?

   (f) What are two components of power dissipation ? Explain in brief.

   (g) What are pull-up and pull-down devices in CMOS circuits ?

   (h) What is the structural gate-level modeling in a CAD tool like VHDL or Verilog ?

   (i) State the different types of VLSI design styles.

   (j) What is meant by fault models ? Give some examples of fault models.

2. (a) Explain the VLSI design flow with a neat diagram. 5

   (b) What are noise margins ? Explain how do noise margins change with increase in the p-transistor width relative to that of n-transistor. 5

3. (a) Consider a non-inverting buffer shown in Figure Q3(a) below that uses an NMOS to pull up and a PMOS to pull down. The NMOS and

PMOS transistors have a threshold voltage $V_{th} = 0.2V$. The supply voltage is $V_{DD} = 1.2\,V$. Determine the transfer characteristics and the regions of operation of the non-inverting buffer. 5

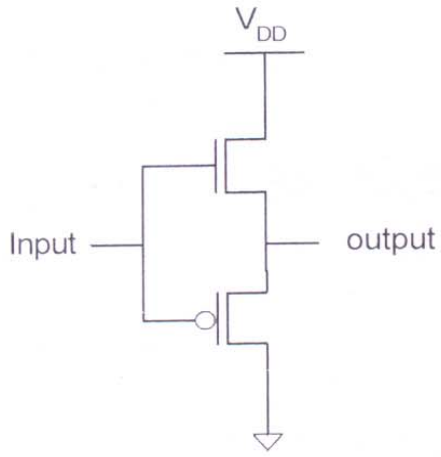

Figure Q3(a)

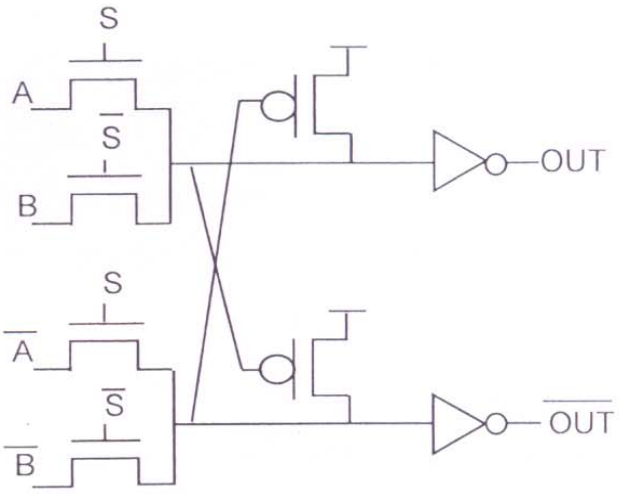

Figure Q3(b)

(b) Why is the cross coupling and PMOS-pull-ups included in the CPL gate shown in Figure Q3(b) above ? What problem are they trying to solve ? 5

4. Derive the CMOS inverter DC characteristics and obtain the relationship for output voltage at different region in the transfer characteristics. 10

5. (a) Draw a transistor level schematic for a CMOS 4-input NOR gate and then sketch a stick diagram for the same. 5

(b) For a CMOS NOR2 gate, prove that if the threshold voltages $V_{Th,n} = |V_{Th,p}|$ and $k_n = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n = k_p = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p$ then, the threshold voltage of the NOR gate is given by $V_{th}\,(NOR2) = \frac{(V_{DD} + V_{Th,n})}{3}$. 5

6. (a) Discuss the charge sharing problems in VLSI circuits. State various circuit techniques in domino CMOS circuits for solving charge sharing problems and explain any one of them. 5

(b) What is pass transistor logic ? Discuss its limitations and design an n-MOS pass transistor which passes weak '1' and strong '0'. 5

7. (a) Consider the two VHDL processes below. How do they differ in terms of functionality ? Be specific. 5

Program 1:

```
PROCESS
BEGIN
WAIT UNTIL ( Clock'EVENT AND Clock = '1' );
IF Reset = '1' THEN
Q2 <= '0';
ELSE
Q2 <= D;
END IF;
END PROCESS;
```

Program 2:

```
PROCESS (Reset, Clock)
BEGIN
IF Reset = '1' THEN
Q3 <= '0';
ELSEIF ( Clock'EVENT AND Clock = '1' ) THEN
Q3 <= D;
END IF;
END PROCESS;
```


(b) Explain BIST with a neat diagram. 5

8. Write short notes any **two** of the following : 5 × 2

(a) P-well process technology

(b) IDDQ testing

(c) CMOS D Latch

(d) Pass Transistor Logic.