Registration No. : | | | | | | | | | | |

Total number of printed pages – 3

B. Tech

PCEC 4401

Seventh Semester (Special) Examination – 2013

VLSI DESIGN

BRANCH : EC, IEE, AEIE, ETC

QUESTION CODE : D 383

Full Marks – 70

Time : 3 Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*

The figures in the right-hand margin indicate marks.

1. Answer the following questions : 2×10

(a) What is standard cell-based design methodology ?

(b) An nMOS transistor has a threshold voltage, $V_{Th} = 0.4$ V and a supply voltage, $V_{DD} = 1.2$ V. A circuit designer is evaluating the proposal to reduce by 100 mV to obtain faster transistor. By what factor would the saturation current increase (at $V_{GS} = V_{Ds} = V_{DD}$) if the transistor were ideal ?

(c) Draw the circuit diagram and the corresponding stick diagram of a 4-input NOR gate using CMOS technology.

(d) What is the minimum power supply voltage required for a CMOS inverter so that it can operate properly ?

(e) Sketch a transistor level schematic for a single-stage CMOS logic for the function $Y = \overline{A \cdot B + C \cdot (A + B)}$.

(f) State two advantages and two disadvantages of complementary logic.

(g) Implement a 2-input NAND gate using pass transistor logic.

(h) What is a tri-state device and what can it be used for ?

P.T.O.

(i) Discuss the solution of cascading problem in the dynamic logic.

(j) In a DRAM what is the main significance to precharge the bit-lines up to $(V_{DD}/2)$ instead of V_{DD} ?

2. (a) Consider a non-inverting buffer shown in Figure Q2(a) below that uses an nMOS to pull up and a *p*MOS to pull down. The *n*MOS and pMOS transistors have a threshold voltage $V_{Th} = 0.2V$. The supply voltage is $V_{DD} = 1.2$ V. Determine the HIGH and LOW voltages at the output and thereby the output swing. 5

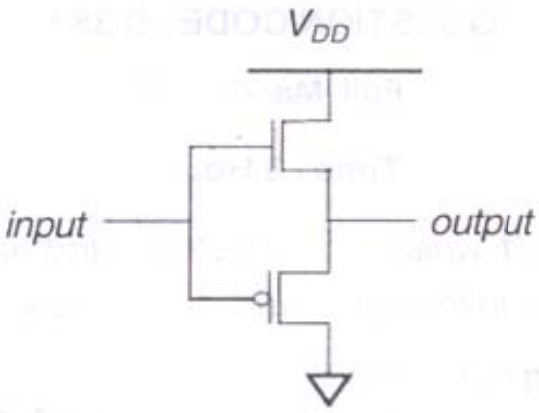

Figure Q2(a)

(b) Why the transient response of the 2-input NOR gate is slower than that of the equivalent inverter? 5

3. (a) Explain the working of an n-channel enhancement type MOSFET after application of gate bias, with the source and substrate at ground potential and the drain-to-source voltage is initially zero. 5

(b) With the help of a neat sketch explain in brief the basic steps of the VLSI design flow. 5

4. What are DC voltage transfer characteristics and noise margins ? How do noise margins change with increase in the p-transistor width relative to that of n-transistor ? Show that for a symmetric CMOS inverter. 10

$$\left(\frac{W}{L}\right)_p \approx 2.5\left(\frac{W}{L}\right)_n$$

5. (a) Give the schematic of XILINX Configurable Logic Block (CLB). 5

(b) Write the VHDL code for a 4-to-1 multiplexer. 5

6. (a) Give a brief description of each of the following terms : 5

(i) HDL

(ii) BIST

(b) State two CAD Tools and describe their use in brief. 5

7. (a) What are the four key DRAM timing parameters ? Write at least two main advantages and disadvantages of DRAM cell ? 5

(b) As a VLSI designer what are the techniques you propose to adopt for reducing active power dissipation in the SRAM cell ? What is gated-V_{DD} structure in CMOS SRAM to reduce leakage current/power ? 5

8 Answer any **two** of the following : 5×2

(a) What is SOI ? What is the material used as insulator ? What are the advantages and disadvantages of SOI process ?

(b) Write the expression for the threshold voltage for a MOS transistor and explain in your own words why the magnitude of the threshold voltage increases as the magnitude of the source-bulk voltage increases (The source-bulk *pn* diode remains reversed biased.)

(c) With the help of a neat circuit diagram show the implementation of the logic function $Y = A + (B + C) \cdot (D + E)$ using domino CMOS logic.

(d) Discuss in brief the fault models for testing of an IC.