Registration No. : | | | | | | | | | | |

Total number of printed pages – 2

B. Tech

FECE 6401

Seventh Semester (Special) Examination – 2013

COMPUTER SYSTEM ARCHITECTURE

BRANCH : AEIE, EC, ETC, IEE

QUESTION CODE : D 428

Full Marks – 70

Time : 3 Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*
The figures in the right-hand margin indicate marks.

1. Answer the following questions : 2×10

   (a) Explain difference between architecture and organization.

   (b) Give one advantage of a direct mapped cache.

   (c) Why is the branch processing unit placed as early in the pipeline as possible ?

   (d) What is an SIMD processor ?

   (e) What is IO mapped input output ?

   (f) What is an interrupt ?

   (g) What is single bus organization ?

   (h) Briefly explain MMU.

   (i) What are the hazards of pipelining ?

   (j) Classify storage devices.

2. (a) Explain block diagram and architecture of common PC. 5

   (b) Define control function in register transfer language. What do you understand by bus transfer ? Explain with examples. 5

P.T.O.

3. (a) Explain message passing architecture in detail. 5

(b) Represent the following conditional control statement by two register transfer statements with control function.

if (P=1) then (R1<– R2)
else if (Q=1) then (R2<– R3)
Draw bus system for above with three stage device. 5

4 What is pipelining ? What is the maximum speed up that can be attained ? Construct an instruction pipeline. Is it possible to attain maximum speed up in an instruction pipeline ? 10

5. (a) Explain various secondary devices. 5

(b) Define register transfer language. What do you understand by arithmetic micro operations ? Explain with examples. 5

6. (a) Briefly explain types of memories used in computer. 5

(b) Explain Booth's algorithm for multiplication of signal 2's complement numbers. 5

7. (a) Explain multithreading in processors. 5

(b) What is content addressable memory ? Describe its design procedure. What is the role of match register. 5

8. Write short notes on any **two** on the following. 5×2

(a) Cache Coherence

(b) SISD

(c) Structural Hazards

(d) RISC vs CISC.