Registration No. : | | | | | | | | | | |

Total number of printed pages – 3

B. Tech

PCEC 4401

Seventh Semester Regular Examination – 2014

VLSI DESIGN

BRANCH(S) : AEIE, EC, ETC, IEE

QUESTION CODE : H 243

Full Marks – 70

Time : 3 Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*

The figures in the right-hand margin indicate marks.

1. Answer the following questions : 2 ×10

(a) What are the advantages of cell-based design methodology ?

(b) Write down an easy-to-use set of design rules for layouts with two metal layers in an ***n***-well process.

(c) Draw the circuit diagram and the corresponding stick diagram of a 3-input NAND gate using CMOS technology.

(d) What is the minimum power supply voltage required for a CMOS inverter so that it can operate properly ? Explain your answer.

(e) Sketch a transistor level schematic of a CMOS 3-input XOR gate. Assume that both the true and complementary versions of the inputs are available.

(f) Write down two advantages and two disadvantages of the pseudo-***n*** MOS logic compared to the CMOS logic.

(g) Implement a 2-to-1 MUX using pass transistor logic and compare this implementation with the transmission gate implementation in terms of number of transistors used in each implementation.

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(h) What is the arrangement in complementary pass transistor logic circuit to reduce the static current due to incomplete turn-off of the ***p***-MOS in the output inverters ?

(i) Briefly describe the difference between a D flip-flop and T flip-flop.

(j) What are the advantages of using address multiplexing scheme in DRAM cell ?

2. Explain the important process sequence for CMOS integrated circuit fabrication with the help of neat diagrams. 10

3. Consider a CMOS process with the device parameters listed below : 10

$\mu_n C_{ox} = 120\ \mu A/V^2$, $\mu_p C_{ox} = 60\ \mu A/V^2$, $V_{Th0,n} = 0.8$ V, $V_{Th0,p} = 1.0$ V, $L = 0.6\ \mu m$ for both ***n***-MOS and ***p***-MOS devices and $W_{min} = 0.6\ \mu m$. Design a CMOS inverter by determining the channel widths W_n and W_p of the ***n***-MOS and ***p***-MOS transistors, to meet the following performance specifications :

- $V_{th} = 1.5$ V for $V_{DD} = 3.0$ V,
- Propagation delay times $\tau^*_{PHL} \leq 0.2$ ns and $\tau^*_{PLH} \leq 0.15$ ns,
- A falling delay $t_{delay} = 0.35$ ns for an output transition from 2.0 V to 0.5 V, assuming a combined output load capacitance $C_{load} = 300\ fF$ and ideal step input.

4. Calculate V_{OL}, V_{OH}, V_{IL}, V_{IH}, NM_L and NM_H for a two-input NOR gate fabricated in a CMOS technology with $(W/L)_p = 4$, $(W/L)_n = 1$, $V_{Thn} = 0.7$ V, $V_{Thp} = -0.7$ V, $k'_n = 40\ \mu A/V^2$, $k'_p = 20\ \mu A/V^2$ and $V_{DD} = 5$ V. 10

5. (a) Starting with the truth table, design a gate level and transistor level clocked JK latch circuit. 5

(b) Draw the basic building block of a CMOS transmission gate dynamic shift register and explain its working. 5

6. (a) Explain with suitable diagrams the data programming and erasing methods in flash memory. 5

(b) Determine whether the leakage current test for chips should be done prior to or after the functional test. What can be said about the test frequency of chips containing dynamic circuits designed to operate at very high

frequency ? Can it fail the functional test at much lower frequency ? If so, explain why ? 5

7. (a) Figure 1 below shows a pass-gate logic network.

(i) Determine the truth table for the circuit. What logic function does it implement ?

(ii) If the PMOS transistor were removed, would the circuit still function correctly ? Does the PMOS transistor serve any useful purpose ? 5

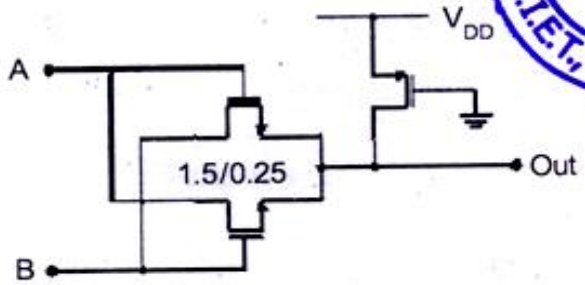

Figure 1

(b) Derive the current equation given by $I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_{Th})V_{DS} - \frac{V_{DS}^2}{2}\right]$ for the MOSFET for which the threshold voltage V_{Th} is not constant but varies linearly with $V(y)$ according to the equation $V_{Th}(y) = V_{Th0} + \alpha V(y)$. 5

8. Answer any two of the following : 5×2

(a) Write a short note on Built-in self-test (BIST).

(b) With the help of a neat sketch show and explain various terms like channel length (L), lateral diffusion length (L_D), and effective channel length (L_{eff}) for a MOS transistor.

(c) Write briefly the limitations of scaling in MOS VLSI design.

(d) Sketch the transistor-level schematics for the basic logic gates INVERTER, AND, OR, XOR using static CMOS and domino logic.