Registration No. : | | | | | | | | | | |

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B. Tech

PCEC 4401

Seventh Semester Back Examination – 2014

VLSI DESIGN

BRANCH (S) : AEIE, EC, ETC, IEE

QUESTION CODE : L 146

Full Marks – 70

Time : 3 Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*
The figures in the right-hand margin indicate marks.

1. Answer the following questions : 2×10

   (a) What is channel-stop implantation ?

   (b) How Power density varies with constant voltage scaling ?

   (c) Draw the schematic diagram of an XOR gate using CMOS Transmission gates.

   (d) Realize AND and NAND logic using CPL.

   (e) Draw the stick diagram of a 2-input NOR gate using CMOS technology.

   (f) What are the stages where a VLSI chip can be tested ?

   (g) What is Dynamic CMOS Logic ?

   (h) What is pseudo logic circuit ?

   (i) What is domino logic ?

   (j) Why does CMOS dissipate power when its input changes from 1 to 0 or from 0 to 1 ?

2. (a) With the help of Band diagram, describe the operation of NMOSFET. 5

   (b) Consider the MOS structure that consists of a p-type doped silicon substrate, a silicon dioxide layer, and a metal (aluminum) gate. The equilibrium Fermi potential of the doped silicon substrate is given as $q\Phi_{Fp} = 0.2$ eV. Using the electron affinity for silicon and the work function for aluminum

given in Figure 1 below, calculate the built-in potential difference across the MOS system. Assume that the MOS system contains no other charges in the oxide or on the silicon-oxide interface. 5

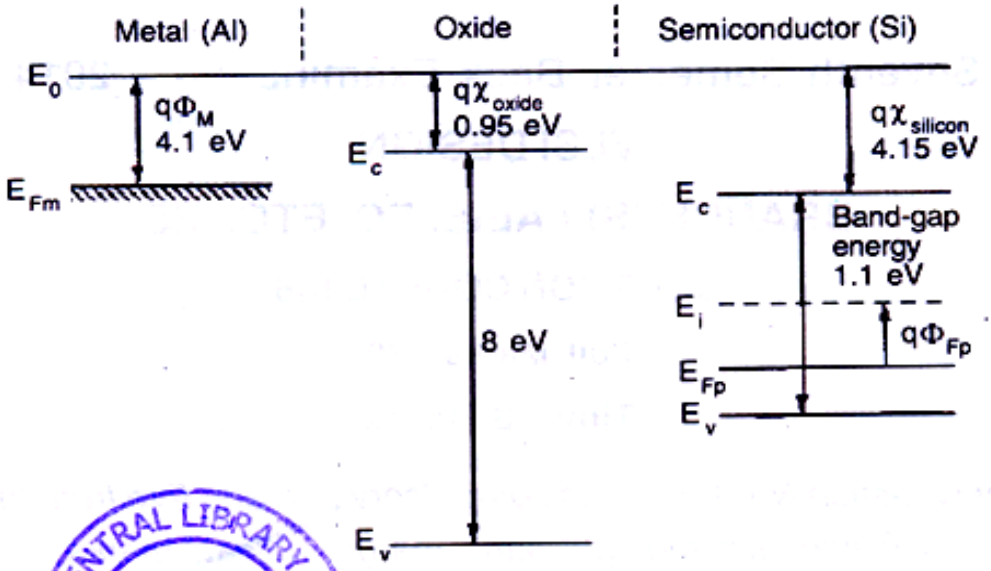

Figure 1

3. Consider the CMOS inverter circuit shown in Figure 2 below, with V_{DD} = 3.3 V. The I-V characteristics of the *n*MOS transistor are specified as follows: when V_{GS} = 3.3 V, the drain current reaches its saturation level I_{Dsat} = 2 mA for V_{DS} = 2.5 V. Assume that the input signal applied to the gate is a step pulse that switches instantaneously from 0 V to 3.3 V. Using the data above, calculate the delay time necessary for the output to fall from its initial value of 3.3 V to 1.65 V, assuming an output load capacitance of 300 *f*F. 10

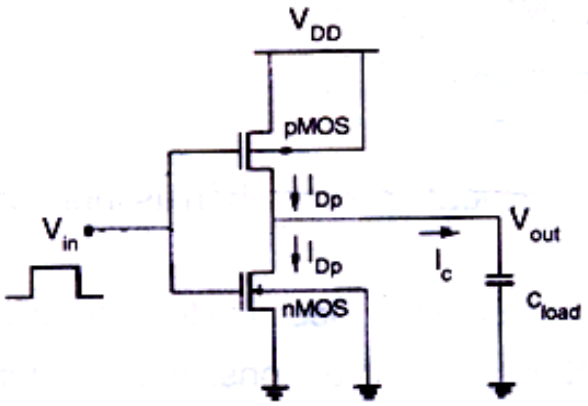

Figure 2

4. A company has access to a CMOS fabrication process with the device parameters listed below :

$\mu_n C_{ox} = 120\ \mu A/V^2$, $\mu_p C_{ox} = 60\ \mu A/V^2$, $V_{TO,n} = 0.8$ V, $V_{TO,p} = -1.0$ V, $L = 0.6\ \mu m$ for both nMOS and pMOS devices and $W_{min} = 1.2\ \mu m$.

Design a CMOS inverter by determining the channel widths W_n, and W_p of the nMOS and pMOS transistors, to meet the following performance specifications.

* $V_{th} = 1.5$ V for VDD = 3 V,
* Propagation delay times $\tau^*_{PHL} \leq 0.2$ ns and $\tau^*_{PLH} \leq 0.15$ ns,
* A falling delay of 0.35 ns for an output transition from 2 V to 0.5 V, assuming a combined output load capacitance of 300 fF and ideal step input. 10

5. (a) For the Boolean expression $Y = \overline{(A + B + C)\cdot(D + E)}$ using CMOS, find the equivalent CMOS inverter circuit for simultaneous switching of all inputs, assuming that $(W/L)_P = 15$ for all PMOS transistors and $(W/L)_N = 10$ for all NMOS transistors. 5

(b) Implement a Full Adder circuit using CMOS. 5

6. (a) Explain how the Transmission Gate transfers both logic '0' and logic '1' efficiently. 5

(b) Implement a 4:1 Multiplexer using Transmission Gates. 5

7. (a) Discuss about FPGA based VLSI design. 5

(b) Describe the operation of four transistor resistive load SRAM cell. 5

8. Write short note on any **two** of the following : 5×2

(a) Constant-Voltage Scaling

(b) Constant-Field Scaling

(c) DIBL

(d) HCI.