Registration No. : | | | | | | | | | | |

Total number of printed pages – 2

B. Tech

PCEC 4401

Seventh Semester Back Examination – 2014

VLSI DESIGN

BRANCH (S) : CSE, EEE

QUESTION CODE : L189

Full Marks – 70

Time : 3 Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*
The figures in the right-hand margin indicate marks.

1. Answer the following questions : 2 ×10

   (a) Why does an NMOS stay in saturation if its gate and drain are shorted together when it is ON state ?

   (b) State two advantages of CMOS inverter over other inverters.

   (c) Why is the Rise time more the than Fall time for a CMOS inverter with NMOS and PMOS of identical physical dimensions and process properties?

   (d) Why does a CMOS inverter dissipate power when its output changes from 1 to 0 or from 0 to 1 ?

   (e) Why is Pull Up Network made by PMOS and Pull Down Network made by NMOS in CMOS based designs ?

   (f) Draw the circuit diagram of a 2-input XOR gate using NMOS Saturation Load.

   (g) Mention two advantages of Dynamic Logic Circuits over Static Logic Circuits.

   (h) State two advantages of SRAM over DRAM.

   (i) What is the difference between Word Line and Bit Line for RAM ?

   (j) State two differences between PROM and EEPROM.

2. (a) Show mathematically, how for Constant Field Scaling, Power Density remains constant even if the scaling factor is changed. 5

   (b) What are the oxide related capacitances in MOSFET ? Calculate the approximate values of oxide related capacitances for cut-off, linear and saturation region for a MOSFET. 5

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3. (a) For a CMOS inverter, derive a mathematical expression for the Threshold Voltage V_{TH} (or Switching Voltage V_{SW}) of the inverter. 5

(b) Show that for a symmetric CMOS inverter i.e. a CMOS inverter for which $V_{in} = V_{out} = 0.5 \times V_{DD}$, it should be true that : $(W/L)_P = 2.5 \times (W/L)_N$. 5

4. (a) Show that the expression for switching (dynamic) power dissipation for a CMOS Inverter is $P = C_{Load} \times V_{DD}^2 \times F$. Here C_{Load} is the output load capacitance; F is the switching frequency of the input signal and V_{DD} is the supply voltage. 5

(b) "PMOS can transfer logic '1' efficiently, but PMOS cannot transfer logic '0' efficiently" – Justify the statement with proper reasoning. 5

5. (a) Implement the logic $Y = \overline{A + B \cdot C}$ using Dynamic CMOS Logic and explain its operation with timing diagram. 5

(b) Implement a 1-bit Full Adder using Transmission Gates. 5

6. (a) Draw the CMOS implementation of basic SR Latch. Explain its operation at MOSFET level. 5

(b) Draw the circuit diagram of NMOS Load (depletion or enhancement) Shift Register and discuss about how it works. 5

7. (a) Draw the circuit diagram of 3 Transistor (3-MOSFET) based DRAM cell and discuss the operation. 5

(b) Design a 2-to-4 NOR based Row Address Decoder Circuit and discuss its operation. 5

8. Write short notes on any **two** of the following : 5×2

(a) Photolithography

(b) LOCOS

(c) Hot Carrier Injection

(d) Built in Self Test.