
Registration no:

Total Number of Pages: 02 **B.TECH**

PCEC4401

7th Semester Regular / Back Examination 2015-16

VLSI DESIGN

BRANCH: AEIE,EC,ETC,IEE

Time: 3 Hours

Max marks: 70

Q.CODE: T188

Answer Question No.1 which is compulsory and any five from the rest.

The figures in the right hand margin indicate marks.

Q1 **Answer the following questions:** **(2 x 10)**

a) Show the basic structure of a MOS transistor.

b) What are the three regions of operation of a MOS transistor**?**

c) What is Body effect?

d) What is the use of the LOCOS technology? Mention its pros and cons.?

e) Define propagation Delay time with suitable illustration.

f) What is the importance of monolithic integration?

g) What are the drawbacks of resistive load inverter? How can they be overcome?

h) Sketch a transistor level schematic of a CMOS 3-input XOR gate. Assume that both the true and complementary versions of the inputs are available.

i) Write down at least two advantages and two disadvantages of the pseudo-***n***MOS logic compared to the CMOS logic.

j) Give the schematic of XILINX Configurable Logic Block (CLB).

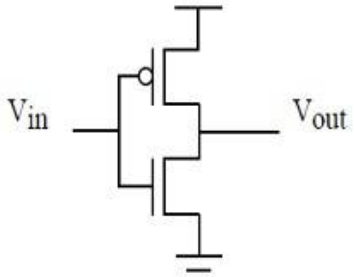
Q2 **a)** Compare the constant field and constant voltage scaling approaches in terms of area, delay, energy and power density parameters. **(5)**

b) Draw a neat sketch of the *Y-chart* (or the Gajski Chart) to illustrate the VLSI design domains. **(5)**

Q3 **a)** What are DC voltage transfer characteristics and noise margins? How do noise margins change with increase in the p-transistor width relative to that of n-transistor? **(5)**

b) Write briefly the limitations of scaling in MOS VLSI design. **(5)**

Q4 Consider the CMOS inverter circuit in Figure Q4 with the following parameters. Assume long channel transistors and no velocity saturation. Given-V_{DD}=3.3 V, k_n=200μA/V^2, k_p=80μA/V^2, V_{T0n}=0.6V, V_{T0p}=0.7V. **(10)**



Find VOL, VOH, VIL, and VIH on the VTC. Also find the noise margins of this inverter.

Q5 **a)** Implement the equation X = ((A'+B') (C'+ D'+E') +F')G' using complementary CMOS using minimum number of transistors. **(5)**

b) A polysilicon trace that is 0.6μm wide, 0.05mm long, and 0.5μm thick has a sheet resistance of 20Ω. It is used to form a high frequency signal trace. **(5)**
i) What is sheet resistance?Calculate the resistance of the poly trace.
ii) Calculate the line capacitance of this signal trace assuming the line is separated from a conducting plate by a 100Å thick oxide layer. Express your answer in fF (10-15)
iii) Calculate the time constant (RC-delay) associated with this trace. What does this result indicate?

Q6 **a)** If a domino gate input is initially a '1' at the start of evaluation, can it make any other transition during evaluation? Why or Why not?Explain briefly, how as a VLSI designer you can optimize the performance of domino logic circuits? Illustrate a domino logic circuit. **(5)**

b) Explain in brief the meanings of regularity, modularity and locality with reference to VLSI design. What is hierarchy in design? **(5)**

Q7 **a)** Draw a 1 T DRAM memory cell. What are the advantages of using address multiplexing scheme in DRAM cell?What are the four key DRAM timing parameters? **(5)**

b) In a DRAM what is the main significance to precharge the bit-lines up to $V_{DD}/2$ instead of V_{DD}?What are the main differences between 1-T DRAM cell and 3-T DRAM cell? **(5)**

Q8 **Write short notes on any two:** **(5 x 2)**

a) CMOS Inverter VTC

b) LOCOS technique

c) BIST

d) CMOS Implementation of SR Latch