Registration no:

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B.Tech
PCEC4401

7th Semester Regular / Back Examination 2016-17

VLSI DESIGN

BRANCH: AEIE, BIOMED, ECE, EEE, EIE, ELECTRICAL, ETC, IEE

Time: 3 Hours

Max Marks: 70

Q.CODE:Y253

Answer Question No.1 which is compulsory and any five from the rest.

The figures in the right hand margin indicate marks.

Q1 **Answer the following questions:** **(2 x 10)**

a) Fill up the columns under NMOS and PMOS with the words "positive" or "negative" appropriately.

Parameters	NMOS	PMOS
Substrate Bias Voltage		
Threshold Voltage		

b) Differentiate between a Short Channel and a Narrow Channel device?

c) Write down at least two advantages and two disadvantages of the pseudo-***n***MOS logic compared to the CMOS logic.

d) Define the terms Modularity and Locality.

e) When is a MOSFET said to operate in Saturation mode?

f) What are the capacitances associated with MOST?

g) Draw the layout diagram of a two input NOR gate.

h) Draw an XOR gate using TG implementation.

i) What is the dynamic power dissipation of a CMOS Inverter? Give the equation.

j) Give the CMOS implementation of a SR Latch.

Q2 **a)** Determine the values of C_{ox} and γ, if $t_{ox} = 22$ Å and $N_A = 3\,X\,10^{17} cm^{-3}$ in a MOST. **(5)**

b) A ***p***-type well in a 130 nm technology has $N_A = 3\times10^{17}$ cm^{-3}. Find the limiting value of depletion layer width and the total charge contained in the depletion region. **(5)**

Q3 **a)** Design a transistor-level CMOS logic circuit to implement the function $F = \overline{(x + yz)(w + x)}$ using the least number of transistors. **(5)**

b) Define the terms rise time, fall time and propagation delay with suitable illustrations. **(5)**

Q4 **a)** What is the Dynamic Logic? What is its drawback? Explain. **(5)**

b) What is Domino CMOS logic? Mention its drawbacks. Give an example. **(5)**

Q5 With the help of suitable diagrams show the fabrication of a CMOS Inverter using the p-tub technology. Name two products that you use in your daily life that you know have used VLSI technology. **(8+2)**

Q6 **a)** Discuss testing Techniques in VLSI. **(5)**

b) Discuss the operating modes of DRAM. **(5)**

Q7 An nMOS transistor has W=4.5µm and L=0.6µm with process parameters k'n = 110 µA/V and Vtn =0.6V. For each of the cases below, identify the region of operation (cutoff, linear, saturation) and calculate the drain current. Assume V = 0V and VDD = 2.2V. **(10)**

a. VGS = 2V, VDS = 1V
b. VGS = 2V, VDS = 2V
c. VGS = 0.5V, VDS = 2V
d. VGS=0.6V, VDS=1V

Q8 **Write short answer on any TWO:** **(5 x 2)**

a) LOCOS technique
b) Energy Band Diagram of MOST
c) FPGA
d) Dynamic Shift Register