GIET UNIVERSITY, GUNUPUR – 765022

Roll No:

Total Number of Pages : 1   AR-19   MCA

MCA 1ST SEMESTER REGULAR EXAMINATIONS, NOV/DEC 2019-20
MCA102-Computer Organization and Architecture

Time: 3 Hours   Max Marks: 70

The figures in the right hand margin indicate marks.

PART- A

Q.1 Answer all of the following: **[10 x 2 =20]**
   a) What is instruction register (IR) and program counter (PC) used for?
   b) What is the mapping procedures adopted in the organization of a Cache Memory?
   c) Explain the concept of pipelining?
   d) What are the two techniques used to increase the clock rate R?
   e) What is 8085 microprocessor?
   f) What do you mean by memory address register (MAR) and memory data register (MDR)?
   g) What are the types of pipeline hazards?
   h) List the various semiconductors RAMs?
   i) What is an I/O Interface?
   j) Define clock rate?

PART-B
[Answer any five out of seven questions]   **[10 X 5=50]**

Q2. (a) Simplify the circuit represented by the following expression using Karnaugh's Map
          F(A, B, C, D)=Σ(1,3,7,8,10,12,14)+d(5,11,15)
   (b) What is flip flop? Discuss the working of R-S flip flop.

Q3.(a) Explain programmed I/o, Interrupt I/o, and DMA.
   (b) What is a Bus? Explain various bus interconnection structures.

Q4. (a) Discuss memory hierarchy in brief. Explain in detail the structure and working of SRAM.
   (b) Discuss the use of a Cache Memory. Explain various cache mapping techniques.

Q5. (a) What are Interrupts? Explain methods for handling interrupts.
   (b) Compare RISC v/s. CISC.

Q6. (a) Draw and Explain Flynn's classification of parallel processing.
   (b) Explain the concept of six stage instruction pipelining? State its effect on conditional branching.

Q7. Write short note on
       (a) Flash Memory
       (b) D- Flip Flop
Q8. Write short note on
       (a) 8085 Microprocessor
       (b) Vector processing