Registration no: | | | | | | | | | | |

Total Number of Pages: 02 **B.Tech**
FECE6401

7th Semester Regular/Back Examination 2017-18
Computer System Architecture
BRANCH: AEIE, ECE, EIE, ETC, IEE
Time: 3 Hours
Max Marks: 70
Q.CODE: B140

Answer Question No.1 which is compulsory and any five from the rest.
The figures in the right hand margin indicate marks.

Q1 **Answer the following questions :** **(2 x 10)**

a) What is a bus? Draw a single bus structure.
b) Differentiate between computer architecture and computer organization.
c) Mention stepwise the control sequence for execution of the instruction Sub (R2),R4.
d) What is a cache? Why it is necessary in computer system?
e) State the difference between Big-endian and Little-endian representation.
f) Give the memory hierarchy of the computer system.
g) State the operation of a call instruction and return instruction in case of subroutine.
h) What do you mean by n-bit ripple-carry adder?
i) State the rules for addition and subtraction for arithmetic operations on floating-point numbers.
j) Mention any four functions performed by system software.

Q2 **a)** Explain the basic Input/output operations with proper diagram. **(5)**

b) Explain branching. How does it differ from straight-line sequencing? **(5)**

Q3 A cache consists of a total of 64 blocks. The main memory contains 4096 blocks , each consisting of 128 words. **(1+3+3+3)**
How many bits are there in a main memory address?
Calculate the no. of bits in tag field, block field and word field for direct mapping.
Calculate the no. of bits in tag field and word field for fully associative mapping.
Calculate the no. of bits in tag field, set field and word field for set associative mapping if one set consists of 4 blocks.

Q4 **a)** Differentiate in detail between RISC and CISC architecture. **(5)**

b) Write the Booth's Algorithm for multiplying two binary numbers in signed 2's complement representation. **(5)**

Q5 **a)** Briefly explain the design of fast adders. **(5)**

b) Discuss in detail about micro programmed and hardwired control unit. **(5)**

Q6 **a)** A virtual memory system has an address space of 8K words, memory space of 4K words and page and block size of 1K words. The following page reference changes occur during a given time interval **(5)**
[4, 2, 0, 1, 2, 6, 1, 4, 0, 1, 0, 2, 3, 5, 7]
Determine the four pages that are resident in main memory after each page reference if replacement algorithm is
FIFO
LRU

b) Explain the concept of memory interleaving with proper diagram. **(5)**

Q7 What do you mean by addressing modes? Explain in detail about the different addressing modes and give an example in each case. **(10)**

Q8 **Write short answer on any TWO :** **(5 x 2)**

a) Assembly language
b) Cache memory vs Virtual memory
c) Fast multiplication
d) Memory management requirement