Registration no: | | | | | | | | | | |

Total Number of Pages: 02 **B.Tech.**
PCEC4401

7th Semester Regular / Back Examination 2017-18
VLSI Design
BRANCH: AEIE, BIOMED, ECE, EEE, EIE, ELECTRICAL, ETC, IEE
Time: 3 Hours
Max Marks: 70
Q.CODE: B240
Answer Question No.1 which is compulsory and any five from the rest.
The figures in the right hand margin indicate marks.

Q1 **Answer the following questions:** **(2 x 10)**

a) State Regularity and Modularity in relevance to VLSI design.
b) What is the difference between positive & negative photoresist.
c) Draw the circuit diagram for function Y = (A.$\bar{B}$ + C).D using CMOS design style.
d) What is the limitation of a nMOS transistor when it is used as a pass transistor?
e) The distance between drain and source diffusion regions is called as-
a) Channel width.
b) Channel length.
c) Channel
d) Gate
f) What is the significance of rise time and fall time.
g) How does the programming of a Flash memory cell is done.
h) List any four electrical faults that can arise in a faulty chip.
i) What types of generators are used to generate test patterns.
j) Draw the voltage transfer curve for two cross-coupled inverters with proper labeling of operating points.

Q2 **a)** Consider a CMOS inverter circuit which contains following parameters V_{DD} = 3.3V, $V_{To,n}$ = 0.6 V, $V_{To,p}$ = -0.7 V, K_n= 200 µA /V^2, K_p =80 µA/V^2. **(5)**
(i)Find the noise margin of the circuit for logic high with proper derivation of parameters.
(ii) Find the noise margin of the circuit for logic low with proper derivation of parameters.

b) Draw and explain the energy band diagrams for a pMOS and nMOS structures operating under inversion and accumulation conditions. **(5)**

Q3 **a)** Consider the following P-channel MOSFET Process. Substrate doping N_D = 10^{15} cm^{-3}, polysilicon gate doping density N_D=10^{20} cm^{-3}, gate oxide thickness t_{ox} = 650 Angstrom and oxide interface charge density N_{ox} = 2 x 10^{10} cm^{-2}, ϵ_{si} = 11.7 ϵ_o and ϵ_{ox} = 3.97ϵ_o for the dielectric coefficient of silicon and silicon dioxide respectively. **(5)**
(a)Calculate the threshold voltage V_{To} for V_{SB} = 0.
Determine the type and amount of channel ion implantation which are necessary to achieve a threshold voltage of V_{To}= -2 V.

b) What do you understand by MOSFET scaling? Describe some of the short channel effects that appear while performing scaling of MOS devices. **(5)**

Q4 **a)** Design a resistive load inverter with R = 1 kΩ, such that V_{OL} = 0.6 V. The enhancement type NMOS driver transistor has the following parameters. **(5)**
V_{DD} = 5 V, V_{To}=1 V, □ = 0.2 $V^{1/2}$, λ = 0, $\mu_n.C_{ox}$ = 22 µA/V^2.
(a) Determine the required W/L.
(b) Determine V_{IL} and V_{IH}.

	b)	What do you understand by the term Minimum Feature Size? Why interconnect delay becomes more dominant when we go for sub-micron CMOS technology circuit designing?	**(5)**
Q5	**a)**	Discuss different levels of deign abstraction with Y- chart.	**(5)**
	b)	Design a 4:1 MUX by using pass transistor logic.	**(5)**
Q6	**a)**	Compare and contrast between pass transistor and transmission gate logic circuit designing.	**(5)**
	b)	Calculate the equivalently W/L of the two nMOSFETs with W1/L and W2/L connected in series. For simplicity, neglect the body effect, i.e., the threshold voltages of individual transistors are constant and do not depend on the source voltages.	**(5)**
Q7		Describe the Precharge& Evaluate logic with regards to Dynamic CMOS logic circuits. What do we do for rectifying the limitation of Dynamic logic circuits?	**(10)**
Q8		**Write short answer on any TWO:**	**(5 x 2)**
	a)	CMOS p-well fabrication process.	
	b)	Semi-Custom VLSIdesign style.	
	c)	Static Random Access Memory(SRAM).	
	d)	Buit- in Self Test(BIST).	