Registration No : | | | | | | | | | | |

Total Number of Pages : 01 **B.Tech**
PCS5I001

5th Semester Regular/Back Examination 2019-20
ADVANCED COMPUTER ARCHITECTURE
BRANCH : CSE
Max Marks : 100
Time : 3 Hours
Q.CODE : HRB225

Answer Question No.1 (Part-1) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.
The figures in the right hand margin indicate marks.

Part- I

Q1 **Only Short Answer Type Questions (Answer All-10)** **(2 x 10)**

a) What do you mean by buffered write through system?
b) What is the difference memory access time and memory cycle time?
c) What do you mean by memory interleaving? Write some advantages of memory interleaving.
d) What do you mean by handshaking mode of data transfer?
e) Differentiate between RISC and CISC?
f) What do you mean by cache Memory?
g) State Amdal's law and explain.
h) What is an Exception in a Pipeline?
i) What are the difference between logical address space and physical address space?
j) What do you mean by cache-coherence?

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 x 8)**

a) Explain in details the working of a micro programmed control unit.
b) How a logical address is mapped to physical address in Virtual Concept?
c) What are the addressing modes available ?Explain with example
d) Write the difference between Random Access Memory and Serially Access Memory.
e) Explain Flynn's Classification.
f) What is a Virtual Memory? Explain with examples.
g) Whether parallelism can be achieved in Uni-Processor System?
h) Explain about Von-Neumann machine.
i) Explain the various phases of an instruction cycles in details.
j) What are the various functions of I/O module?
k) Explain Booth's multiplication algorithm with the help of an example.
l) What is meant by "Locality of reference "and how does it help in faster execution of the program.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 Differentiate between super scalar architecture Vs super pipelined architecture. **(16)**

Q4 How do you mean by pipeline Hazard? How control hazard is detected and resolved? Explain with time-space diagram. **(16)**

Q5 Explain how data may be transferred from hard disk to memory using DMA including arbitrations for the Bus. **(16)**

Q6 Differentiate between static data flow and dynamic data flow in computer system with example. **(16)**