Registration No :

Total Number of Pages : 02

B.Tech

PEE5I102

5th Semester Regular / Back Examination 2019-20
MICROPROCESSOR & MICROCONTROLLER
BRANCH : ELECTRICAL
Max Marks : 100
Time : 3 Hours
Q.CODE : HRB163

Answer Question No.1 (Part-1) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.

The figures in the right hand margin indicate marks.

Part- I

Q1 Only Short Answer Type Questions (Answer All-10) **(2 x 10)**

a) List out the control and status signal lines available in 8085

b) What is the difference between RET and RETI instructions?

c) One user transfer an ASCII character “E” (45H) with no parity bit, one start bit, one stop bit. Find the time take to transfer 1000 characters using 9600 bps.

d) If carry=1& A=75H and B=3FH prior to execution of SUB A,B , then what will be the content of A after execution.

e) Assume the contents of accumulator are 71H and CY=0.Illustarate the accumulator content after RRC and RAR instructions.

f) Distinguish between interrupt and polling.

g) What is the significance of ALE pin in 8051?

h) Distinguish between RISC processor and CISC processor.

i) To get a 20 μs delay, which value should be loaded into TH register using mode 1 , where XTAL=11.0592 MHz.

j) Determine the control word of 8255 PPI, when port A=out put, port B=output, port C_{lower}=input, port C_{upper}=input.

Part- II

Q2 Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) **(6 x 8)**

a) Explain the various steps of instruction decoding and execution in 8085.

b) Write a program to transfer the bytes of ROM space into RAM location starting at 50H. Assume that ROM space starting at 400H contains “BPUTODISHA” .

c) Draw the timing diagram for execution of the instruction MVI A, 54H

d) Write a subroutine to generate delay of 220 ms. Assume crystal frequency = 12 MHz.

e) How does data transfer from memory to microprocessor occurs? Explain in detail.

f) Describe all steps of interrupt process of 8085.

g) Do the schematic diagram to show the minimum interface between a computer and a peripheral.

h) What do you meant by stack and bank1 conflict with reference to their address in 8051? What steps are being followed to overcome this problem?

- **i)** Assume that we have 4 bytes of hexadecimal data: 35H, 42H, 3FH, and 52H.
  - (a) Find the checksum byte,
  - (b) perform the checksum operation to ensure data integrity,
  - (c) if the second byte 42H has been changed to 22H, show how checksum detects the error.
- **j)** Assume that the lower three bits of P1 are connected to three switches. Write a program to send the ASCII characters 0,1,2,3,4,5,6,7 based on the status of the switches.
- **k)** How direct memory data transfer occurs in 8085? Discuss using suitable figure.
- **l)** Write a program to read 200 bytes of data from P1 and save the data in external RAM staring at RAM location 3000H.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 Draw the block diagram of the 8259 and explain how it can be used for increasing the interrupt capabilities of 8085. Explain how 8259 read the status and change the interrupt mode during a program execution. **(16)**

Q4 Describe the internal hardware architecture of Intel 8086 in details using suitable schematics. **(16)**

Q5 Write an assembly language program to divide one 16 bit number with an 8 bit number in 8085 **(16)**

Q6 Draw and explain the architecture details of 8051 and discuss the different addressing modes of 8051. **(16)**