Registration No : | | | | | | | | | | |

Total Number of Pages : 02 **B.Tech**
PET5H002

5th Semester Regular / Back Examination 2019-20
DIGITAL VLSI DESIGN
BRANCH : ECE, ETC
Max Marks : 100
Time : 3 Hours
Q.CODE : HRB299

Answer Question No.1 (Part-1) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.
The figures in the right hand margin indicate marks.

Part- I

Q1 **Only Short Answer Type Questions (Answer All-10)** **(2 x 10)**

a) State the advantages offered by monolithic integration.
b) Why the concept of locality is important in vlsi designing of ICs.
c) Draw the stick diagram for a XOR2 gate.
d) Draw Y-chart representing the various domains of VLSI design flow.
e) What is the significance of LOCOS in VLSI chip fabrication.
f) What is the reason behind development of built-in potential in a MOS system?
g) What do you understand by high to low and low to high delay times? Are their values equal. why?
h) Write the differences between static and dynamic circuits.
i) Draw the circuit diagram for a negative edge triggered D-flip flop using transmission gates.
j) What advantages does Built-In Self Test offers over other testing techniques?

Part- II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 x 8)**

a) Explain the concept of design hierarchy with the help of a suitable example.
b) For a CMOS n-well process, illustrate the steps for fabrication of a CMOS inverter.
c) Draw a neat and properly labelled layout of an NAND2 gate using pseudo NMOS design style.
d) Derive the equation for depletion region width in a MOS system when it is applied with an external bias.
e) Given V_{DD} = 5 V, k_n' = 30 $\mu A/V^2$, and V_{To}= 1 V, design a resistive-load inverter circuit with V_{OL}= 0.2 V. Specifically, determine the *(WIL)* ratio of the driver transistor and the value of the load resistor R_L that achieve the required V_{OL}.
f) Describe about the static and dynamic power dissipation in vlsi circuits.
g) Implement a XOR3 gate in CMOS design style.
h) What are the limitations of using independent pass transistors? Implement $Y = (A + B).(\bar{B} + C.D)$ in Pass transistor logic.
i) Implement the logical equation $Y = (\bar{B} + C.A)$ in CMOS, pass transistor and transmission gate logic.
j) With the help of suitable diagram explain about domino circuits. Mention the characteristics of these circuits.
k) Explain about the different types of fault types and models useful in testing of VLSI chips. Support your answer with proper diagrams.
l) With suitable diagrams explain the reading and writing operations for a SRAM(Static Random Access Memory) cell.

Part-III

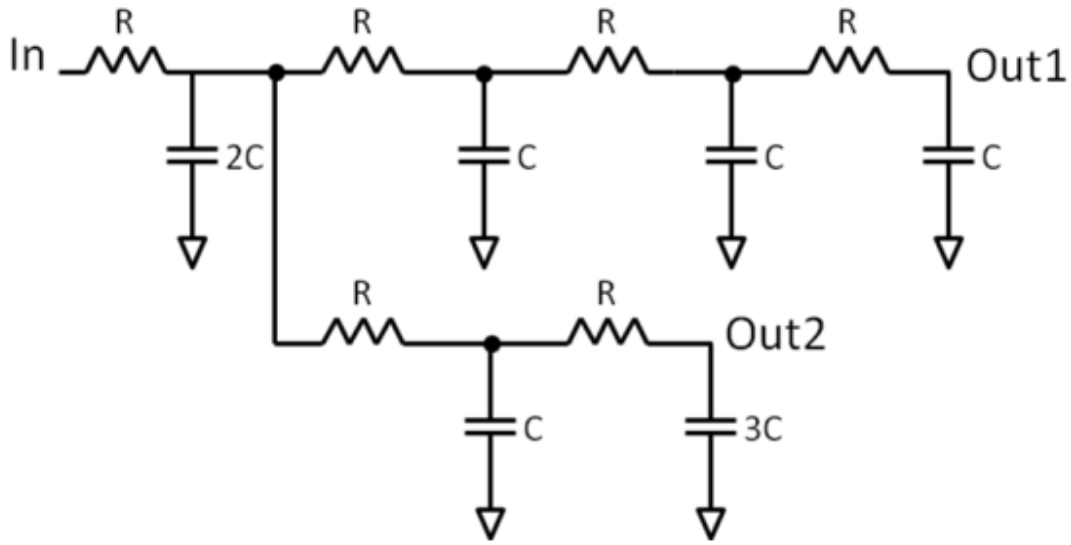
Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 **a)** Why mask layouts are of much importance in VLSI IC fabrication. **(8)**

b) Compare and contrast between lambda and micron layout design rules. **(8)**

Q4 **a)** Explain about Elmore delay model used for finding delay in the circuit branches. **(8)**

b) For the below circuit, with R = 100 ohm and C = 10 femto Farad, calculate the Elmore delay from In to Out1 and Out2. Which path is critical path. **(8)**



Q5 **a)** Write a detailed note on True Single Phase Clocked Register(TSPCR) ciruits. **(8)**

b) Consider a CMOS inverter circuit which contains following parameters : **(8)**

V_{DD} = 3.3V, $V_{To,n}$ = 0.6 V, $V_{To,p}$ = -0.7 V, K_n = 200 µA /V^2, K_p = 80 µA/V^2.

(a) Find the noise margin of the circuit for logic high with proper derivation of parameters.

(b) Find the noise margin of the circuit for logic low with proper derivation of parameters.

Q6 **a)** How does DRAMs(Dynamic RAM) are able to provide a higher packing density as compared to SRAMs? Explain. **(5)**

b) What is the clock overlap condition in C^2MOS circuits? Describe the situation for a (1,1) clock overlap case with suitable diagram. **(5)**

c) What function does a PRPG(Pseudo Random Patten Generator) perform in testing of VLSI ICs. **(6)**