



Registration No:

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Total Number of Pages : 2

AR-17

B.TECH

B.TECH 5th SEMESTER EXAMINATIONS, NOV/DEC 2019
BEEPC5030 MICROPROCESSOR AND MICROCONTROLLER
 EEE BRANCH

Time : 3 Hours

Maximum : 100 Marks

Answer ALL Questions

The figures in the right hand margin indicate marks.

PART – A: (Multiple Choice Questions) 10 x 2=20 MarkQ.1. Answer All Questions

- | | | |
|---|---|-------------|
| a | The clock frequency of 8085 Microprocessor is
a) 5 MHz b) 3 MHz c) 6 MHz d) 8 MHz | [CO1] [PO1] |
| b | In 8085 Microprocessor the address and data buses are distinguished using
a) HOLD b) READY c) ALE d) S ₁ | [CO1] [PO1] |
| c | The highest priority interrupt in 8085 Microprocessor is
a) INTR b) RST 7.5 c) RST 5.5 d) TRAP | [CO1] [PO1] |
| d | In Microprocessor which signal is used for accessing DMA operation is
a) ALE b) INTR c) HOLD d) S ₀ | [CO1] [PO1] |
| e | To select a whole word in 8086 memory the status of A ₀ and /BHE is
a) 0 and 0 b) 1 and 0 c) 1 and 1 d) 0 and 1 | [CO2] [PO1] |
| f | How many operating modes are there in 8086 Microprocessor
a) 3 b) 2 c) 4 d) 1 | [CO1] [PO2] |
| g | The DPTR in 8051 Microcontroller is how many bits
a) 8 bits b) 16 bits c) 32 bits d) 64-bits | [CO2] [PO1] |
| h | The internal RAM size of 8051 Microcontroller is
a) 256 byte b) 512 byte c) 128 byte d) 1024 byte | [CO4] [PO1] |
| i | The number of channels in 8257 DMA controller is
a) 2 b) 3 c) 4 d) 5 | [CO3] [PO1] |
| j | How many counters are available in 8254 PIT
a) 2 b) 3 c) 4 d) 5 | [CO3] [PO1] |

PART – B: (Short Answer Questions) 10X2=20 MarksQ.2. Answer All questions

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|---|---|-------------|
| a | Distinguish between FETCH and EXECUTE Cycle. | [CO1] [PO1] |
| b | What is the maximum memory size that can be addressed by 8085 Microprocessor? Justify. | [CO2] [PO1] |
| c | What is the role of signals S ₁ and S ₀ in 8085 Microprocessor? | [CO1] [PO1] |
| d | What is the significance of FFFF0H in 8086 Microprocessor? | [CO2] [PO2] |
| e | Explain the operation of Direction Flag and Trap Flag in 8086 Microprocessor. | [CO2] [PO1] |
| f | Distinguish between single and multiprocessor mode in 8086 microprocessor. | [CO1] [PO1] |
| g | State the register Banks in 8051 microcontroller. | [CO4] [PO1] |
| h | State the Conflict between stack and Bank1 in 8051 microcontroller. | [CO4] [PO1] |
| i | What is the function of A ₀ and A ₁ in 8255 PPI? | [CO3] [PO1] |
| j | Write down the control word content of 8255 in I/O mode, mode-0 to initialize Port-A as input, Port-B as output and Port-C is not used. | [CO3] [PO1] |

PART – C: (Long Answer Questions) 4X15=60 MarksAnswer All questions

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|-----|---|----|-------------|
| Q.3 | | | |
| a | Explain the register organization of 8085 Microprocessor. | 8 | [CO1] [PO1] |
| b | Explain the instruction cycle of 8085 Microprocessor. | 7 | [CO2] [PO1] |
| | OR | | |
| c | Explain the internal architecture of 8085 Microprocessor. | 10 | [CO1] [PO1] |
| d | Explain the addressing modes in 8085 Microprocessor. | 5 | [CO2] [PO1] |
| Q.4 | | | |



- a Briefly explain the maximum mode Signals of 8086 Microprocessor. 7 [CO1] [PO1]
- b Explain the following instructions of 8086 Microprocessor 8 [CO2] [PO1]
a) XCHG b) LEA c) CBW d) LAHF
- OR
- c Explain the minimum mode system timing diagram in 8086 Microprocessor. 7 [CO1] [PO1]
- d Explain the following signals of 8086 Microprocessor 8 [CO2] [PO2]
a) $\overline{MN}/\overline{M\overline{X}}$ b) READY c) HOLD d) DT/\overline{R}
- Q.5
- a Explain the I/O and BSR mode of 8255 PPI. 8 [CO3] [PO1]
- b Explain the interfacing of 8255 with 8086 Microprocessor. 7 [CO3] [PO1]
- OR
- c Explain the priority schemes in 8257 DMA controller. 8 [CO3] [PO1]
- d Explain the mode register in synchronous and asynchronous mode of 8251. 7 [CO3] [PO1]
- Q.6
- a Explain the block diagram of 8051 Microcontroller. 8 [CO4] [PO1]
- b Describe the RAM organization in 8051 Microcontroller. 7 [CO4] [PO1]
- OR
- c Explain the Timer/counter module in 8051 Microcontroller. 10 [CO4] [PO1]
- d Explain the interrupts in 8051 Microcontroller. 5 [CO4] [PO1]

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