Registration No : | | | | | | | | | | |

Total Number of Pages : 02 **B.Tech**
PCS3I101

3rd Semester Back Examination 2019-20
SWITCHING THEORY & LOGIC DESIGN
BRANCH : CSE
Max Marks : 100
Time : 3 Hours
Q.CODE : HB601

Answer Question No.1 (Part-1) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.
The figures in the right hand margin indicate marks.

Part-I

Q1 **Only Short Answer Type Questions (Answer All-10)** **(2 x 10)**

a) Convert $(95.5)_{10} = (?)_{16}$
b) Assume the number $(10011001)_2$ in 2's complement representation. What will be the decimal equivalent of the number?
c) Express the given function in sum of minterms form. F(x, y, z) = 1
d) Given $F_1 = \sum m$ (0, 1, 3, 6) and $F_2 = \sum m$ (0, 2, 4, 6). What is the miterm expansion of F_1F_2?
e) Write is the advantages of tabulation method?
f) List the applications of Multiplexer.
g) What is meant by priority encoder? How is it different from encoder?
h) Write the difference between static and dynamic hazards.
i) A MOD-16 counter clocked by 10 KHz clock signal. Find the frequency at the output of MSB.
j) How an ASM chart different from general flow chart?

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 x 8)**

a) The seven bit even parity Hamming code 0011011 received through a noisy channel. Decode the message assuming that at most a single error has occurred in code word.
b) If $\mathbf{Z = \overline{X}Y + X\overline{Y}}$, then show that $\mathbf{\overline{X}Z + X\overline{Z} = Y}$
c) Simplify the expression using boolean algebra.
$\mathbf{F(X,Y,Z) = (\overline{X} + Y)(X + Y + Z)\overline{Z}}$
d) Minimize the boolean function using K-Map.
$\mathbf{F(A,B,C,D) = \prod M(1,2,3,8,9,10,11,14).d(7,15)}$
e) How a full adder different from a half adder? Design a full adder using NAND gate only.
f) An 8 to 1 MUX has inputs A, B and C connected to the selection inputs S_2, S_1 and S_0 respectively. The data inputs D_0 through D_7 are as follows $D_0=D_2=D_5=D_7=1$; $D_3=D_6=0$; $D_2=D_4=D$. Determine the boolean expression that the MUX implements.
g) Distinguish between static-0 and static-1 hazard. Find a circuit that has no static hazards and implement the boolean function. $\mathbf{F(x,y,z) = \sum m(1,5,6,7)}$
h) Construct a 5 to 32 line decoder with four 3 to 8 line decoders with enable and a 2 to 4 line decoder. Use block diagram for the components.
i) Show that the characteristic equation for the complement output of a JK flip flop is
$\mathbf{Q'(t+1) = J'Q' + KQ}$

j) Design a 4-bit shift register with parallel load using D-flip flops. There are two control inputs: shift and load. When shift=1 and load=0 the content of the register is shifted by one position. New data is transferred to the register when load=1 and shift=0. If both control inputs are equal to 0, the content of the register does not change.

k) Assume that 1011 input data pattern is loaded into a 4-bit ring counter. Sketch the resulting flip flop Q output waveforms (assuming positive edge triggering).

l) Draw the ASM chart for a sequential circuit having two D-FF and one input x. when x=0, the state of the circuit remains the same. When x=1, the circuit goes through the state transition from 00 to 01 to 11 to 10 back to 00 and repeats.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 Simplify the following four variable Boolean function using Quine-Mcclusky method. **(16)**

$$F(A,B,C,D) = \sum m(1,3,5,10,11,12,13,14,15)$$

Q4 **a)** Implement a full subtractor using demultiplexer. **(8)**

b) Design a 4-bit by 3-bit binary multiplier using 4-bit added and necessary gates. **(8)**

Q5 Design a synchronous 3-bit binary UP/DOWN counter. Consider a variable X and when X= "0", it will count from "000" to "111" and when X= "1" it will count from "111" to "000" using T- FF. **(16)**

Q6 A sequential circuit with two D-FF A and B, two inputs X and Y and one output Z. The specified next state and output equation as given below: **(16)**

$$A(t+1) = x'y + xA$$

$$B(t+1) = x'B + xA$$

$$Z = B$$

(i) Draw the logic diagram of the sequential circuit.
(ii) Draw the state table for the sequential circuit.
(iii) Draw the corresponding state diagram.
Using this state equation design the circuit with JK Flip-flop.