GIET MAIN CAMPUS AUTONOMOUS GUNUPUR – 765022

RN19001865

Registration No: | | | | | | | | | | |

Total Number of Pages : 2 AR-18 B.TECH

B.TECH 3rd SEMESTER EXAMINATIONS, NOV/DEC 2019

BECES3030 DIGITAL LOGIC DESIGN

Common to CSE/IT

Time : 3 Hours Maximum : 100 Marks

Answer ALL Questions

The figures in the right hand margin indicate marks.

PART – A: (Multiple Choice Questions) 10 x 2=20 Mark

Q.1. Answer *All* Questions

a What is the minimum number of two-input NAND gates used to perform the function of two input OR gate ?

i 1. ii 2 iii 3 iv 4

b The number of full and half-adders required to add 16-bit numbers is

I. 8 half-adders, 8 full-adders
II. 1 half-adder, 15 full-adders
III. 16 half-adders, 0 full-adders
IV. 4 half-adders, 12 full-adders

c The sum of 11101 + 10111 equals _____.

i) 110011
ii) 100001
iii) 110100
iv) 100100

d **Which of the following expressions is not equivalent to X ' ?**

I. X NAND X
II. X NOR X
III. X NAND 1
IV. X NOR 1

e Simplified form of the Boolean expression (X + Y + XY) (X + Z) is

I. X + Y + Z
II. XY + YZ
III. X + YZ
IV. XZ + Y

f The resolution of an *n* bit DAC with a maximum input of 5 V is 5 mV. The value of *n* is

I. 8
II. 9
III. 10
IV. 11

g In the expression A + BC, the total number of minterms will be

I. 2
II. 3
III. 4
IV. 5

h Which of the following is non-saturating?
- I. TTL
- II. CMOS
- III. ECL
- IV. Both I and II

i A mod-2 counter followed by a mod-5 counter is
- I. Same as a mode-5 counter followed by a mod- 2 counter
- II. A decade counter
- III. A mod-7 counter
- IV. Ripple carry Counter

j A J-K lip-lop has its J-input connected to logic level 1 and its input to the Q output pulse is fed to its clock input the flip-flop will now
- I. Change its state at each clock pulse
- II. Go to state 1 and stay there
- III. Go to state 0 and stay there
- IV. Retain its present state

PART – B: (Short Answer Questions) 10X2=20 Marks

Q.2. Answer *ALL* questions

a What is gray code? Convert $(100110101)_2$ into gray code.

b Implement the logic expression AB+C using two input NOR Gates only. Use minimum number of gates.

c Draw the logic diagram of 1:16 DEMUX using 1:4 DEMUX

d Implement the function F = ∑ m (2,3,5,7,8,9,12) using 8:1 Multiplexer.

e Find the complement of $F = x + yz$; then find the values of F.F' and F + F'.

f Construct a J-K Flip Flop using a D Flip Flop.

g Draw the Circuit of a TTL Nor gate.

h Implement the logic F = ∑(m1, m4, m6, m8, m9, m9,m11) using a suitable decoder.

i An 8 bit DAC has a full scale output of 2 mA and full scale error of ± 0.5%. If input is 10000000 find the range of outputs.

j Write the excitation table for T and R-S flip flops.

PART – C: (Long Answer Questions) 4X15=60 Marks

Answer *ALL* questions

Q.3

a Formulate a Weighted binary code for the decimal digits using the following weights 7
I . 6,3,1,1 II . 6, 4, 2, 1

b For the Boolean Expression F = xy'z + x'y'z + w'xy + wxy 8
- i. Use the Boolean algebra to simplify the function to a minimum number of literals
- ii. Obtain the function F as the sum of minterms from the simplified expression and draw the logic diagram.

OR

c Given X = 1101010 Y = 0101011. Find X-Y and Y-X using 1's complement and 2's complement. 7

d Implement the X-OR, X-NOR logic using 8
i. NAND gates only ii. NOR gates only

Q.4

a In a tabular form, write the "2421" code and "Excess-3" code of decimal digit "0 to 9". What are the special properties of these codes? 8

b Construct a 32:1 MUX using multiple 8:1 MUX and 4:1 MUX. 7

OR

c Design a 8421 BCD adder circuit. 7

d Design a 2 bit comparator using a suitable decoder. 8

Q.5

a A sequential circuit with two D-flip flops *A* and *B*, two inputs *x* and *y* and one output *z* is specified by the following equations *A(t+1) = x'y + xA, B(t+1) = xA + x'B, z = B* . Draw the logic diagram of the cuircuit. List the state table and draw the state diagram. 7

b Design a synchronous counter that has the following sequence: 000, 011, 111, 101,110 and repeats itself. The undesired (unused) states 001, 010, and 100 must always go to 000 on the NEXT clock pulse. 8

OR

c Write short note on Parallel In Serial Out Shift Register 7

d Design a four bit binary synchronous counter with D flip flops. 8

Q.6

a Design a circuit to find square of a 3 bit number using a ROM. 7

b Design a CMOS Inverter 8

OR

c A ROM chip of 4096 x 8 bits has two chip select input and operates from a 5 V power supply. How many pins are needed for integrated circuit package. Draw a block diagram, and label all input and output terminals in the ROM. 7

d Explain the operation of a Dual slope A/D converter with neat diagram. 8

==0==