Registration no:

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B.Tech
PCEL4303

6th Semester Regular / Back Examination 2016-17
MICROPROCESSOR AND MICROCONTROLLER
BRANCH(S): CSE, ELECTRICAL
Time: 3 Hours
Max Marks: 70
Q.CODE: Z126

Answer Question No.1 which is compulsory and any five from the rest.
The figures in the right hand margin indicate marks.

Q1 **Answer the following questions:** **(2 x 10)**

a) What is the need of two memory banks in 8086 Microprocessor? Which part of data bus is connected to ODD bank and which part is connected to EVEN bank?

b) 8086 Microprocessor is to be operated at 5.2MHz. What should be the crystal frequency which is to be connected to 8284's clock generator?

c) What is the word length and physical address capacity of the 8085 and 8086 microprocessors?

d) State two differences between 8085 and 8086 microprocessor.

e) In How many modes 8255PPI's port A can be configured?

f) Explain the difference between AND & TEST instructions of 8086?

g) Assume that DF = 1, SI = 0010H and DI = 0020H. What will be the content of SI and DI after executing MOVSW instruction?

h) What is the role of a segment register in the protected mode of 80386 Microprocessor?

i) How many registers banks are there in 8051? Which bank is used for stack?

j) The data transfer across an asynchronous serial data communication line is observed and the bit time is measured as 0.625ms. What is the baud rate?

Q2 **a)** Explain the 8085 Microprocessor architecture with the help of block diagram. **(5)**

b) Explain the different status and control flags of 8086 Microprocessor. **(5)**

Q3 **a)** Explain the different addressing modes of 8086 Microprocessor with the help of examples. **(5)**

b) How many counters are there in 8254? Which mode is to be used in order to generate a square wave? What value should be loaded in the counters count register in order to generate square wave of 1KHz if the counter is operating at 1.45MHz? **(5)**

Q4 **a)** Draw and explain the read bus cycle of 8086 Microprocessor. **(5)**

b) How 64 peripheral devices can be connected in Cascaded mode/Master-Slave mode of 8259 Programmable Interrupt controller? Explain with the help of neat diagram. **(5)**

Q5 **a)** Write an 8086 assembly language program in order to perform block transfer. Assume that the offset address of the source is 1000H and offset address of the destination is 2000H and block size is 50 bytes. [Use string related instructions while writing the program]. **(5)**

b) Differentiate between SUB & CMP and MOV & LEA instructions of 8086 Microprocessor. **(5)**

Q6 **a)** Explain about the internal RAM organization of 8051 Microcontroller. **(5)**

b) Explain the register organization of 80386 Microprocessor. **(5)**

Q7 Draw the block diagram of 8255 PPI. Explain the I/O control word and BSR control word. Write initialization instructions to configure Port A as input port, Port B as output port, PC_L as input port, PC_U as output port. Assume that the port address of control register is OOFFH. **(3+4+3)**

Q8 **Write short answer on any TWO:** **(5 x 2)**

a) 8251 USART

b) Rotate instructions of 8086 [ROR, ROL, RCR, RCL]

c) Maximum mode of 8086

d) DAC interface with 8086