Registration No : | | | | | | | | | | |

Total Number of Pages : 02 **B.Tech**
PCS5I001

5th Semester Regular Examination 2017-18
Advanced Computer Architecture
BRANCH : CSE
Time : 3 Hours
Max Marks : 100
Q. CODE : B310

Answer Question No.1 and 2 which are compulsory and any four from the rest.
The figures in the right hand margin indicate marks.

Q1 **Answer the following questions*: multiple type or dash type*** **(2 x 10)**

a) 80386 Microprocessor is ____bit processor.
b) In Super Scalar architecture instruction scheduling is
i)Static ii) Dynamic iii) Hybrid iv) Pseudostatic
c) Array Processor is
i)SISD ii) MISD iii) SIMD iv) MIMD
d) The number of Control Units in Vector Processor is
i)one ii) two iii) four iv) n
e) Bisection width of N X N mesh network is _____.
f) The number of switches required for N X N Dynamic network is_____.
g) Type of memory used in set-associative cache is
i)Static ii) Dynamic iii) Associative iv) Pseudostatic
h) The technique used in Virtual memory is
i)paging ii) segmentation iii) either (i) or (ii) iv) both (i) and (ii)
i) Type of control unit used in RISC is
i)Hard-wired ii) Soft-wired iii) Microprogrammed iv) both (i) and (ii)
j) Memory bus is
i)Synchronous ii) Asynchronous iii) Semi-synchronous iv) both (i) and (ii)

Q2 **Answer the following questions: *Short answer type*** **(2 x 10)**

a) What do you mean by Spatial and Temporal locality of reference?
b) What is Flynn's classification?
c) What do you mean by Cache coherence?
d) What do you mean by Address space?
e) Whether for single instruction execution non-pipeline system is better than pipeline system? Justify.
f) What do you mean by Distributed memory system?
g) How many Floating point registers are there in the Floating Point Unit of SPARC?
h) How overlapped CPU and I/O operations are performed in computer system? Explain with example.
i) State Amdahl's low and explain.
j) To multiply 18 by -1, if 18 is in source, how many cycles needed by ARM?

Q3 **a)** Assume a cache miss penalty is 100 clock cycles, and all instructions take 1.0 clock cycles. Let the average miss rate is 2%, there is an average of 1.5 memory references per instructions, and the average number of cache misses per 1000 instructions is 30. What is the impact on the performance and calculate the impact using both misses per instruction and miss rate? **(10)**
b) What are the writing policies of Cache? Explain with diagram. **(5)**

Q4 **a)** What do you mean by Speed-Up of pipeline? Derive equations of Speed-Up and Efficiency for Pipeline, Super pipeline and Super scalar architecture. **(8)**
b) What is a SPARC processor? What are the modules in SPARC? Explain each. **(7)**

Q5	**a)**	What is a Pipeline Hazard? How control hazard is detected and resolved? Explain with example.	**(10)**
	b)	What is THUMB? How THUMB instructions are executed by ARM? Is it advantageous?	**(5)**
Q6		Distinguish and Differentiate.	
	a)	UMA Vs. NUMA	**(5)**
	b)	RISC Vs. CISC	**(5)**
	c)	Super scalar architecture Vs. VLIW architecture	**(5)**
Q7	**a)**	What is Interconnection network? Draw a Shuffle network and explain the communication mechanism.	**(10)**
	b)	Whether array processor is same as vector processor? Justify your answer.	**(5)**
Q8	**a)**	What is virtual memory? How a logical address is mapped to physical address in virtual concept? Explain with example and diagram.	**(10)**
	b)	What are the page replacement algorithms are used in virtual memory? Explain each.	**(5)**
Q9		**Write Short Notes on any THREE.**	**(5 x 3)**
	a)	Distributed memory system	
	b)	I/O subsystem	
	c)	Cloud computing	
	d)	Microcontroller	