Registration No. : | | | | | | | | | | |

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B. Tech

PCCS 4301

Fifth Semester Examination – 2013

COMPUTER ORGANIZATION

BRANCH : IT, CSE

QUESTION CODE : C-333

Full Marks – 70

Time : 3 Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*
The figures in the right-hand margin indicate marks.

1. Answer the following questions : 2×10

(a) What is Von Neumann concept ?

(b) In Implied addressing mode how many memory reference required for execution of an instruction ?

(c) What is Zero-address instruction format? Explain with proper example.

(d) What do you mean by Dynamically programmable control unit ?

(e) What is Response time and Data transfer time of a disk ?

(f) Find the 2's complement of the following binary strings, which are in signed magnitude binary number representation.

0 0000 0 1001 0 1111 1 0000

(g) What do you mean by Single accumulator organization? Explain with an example.

(h) What is Nested subroutine? How Stack is used for return address ?

P.T.O.

(i) What are the functions of following registers ?

IP, SP, PC, MAR

(j) Draw the flow diagram for unsigned binary number multiplication.

2. Distinguish and differentiate : 2.5×4

(a) Vertical micro-instruction vs. Horizontal micro-instruction

(b) Big-endian vs. Little-endian

(c) Temporal locality of reference vs. Spatial locality of reference

(d) Address space vs. Memory space.

3. Justify your answer : 2.5×4

(a) Whether Control bus is bidirectional ?

(b) Is IR register same as IP register ?

(c) An instruction with an indexed operand having address field with all bits are 0 is effectively a register indirect mode of operation.

(d) Can we replace RAM with Cache ?

4. a) In an 11 bit computer instruction format the size of the address field is 4 bits. The system uses expanded opcode technique. It has 5 two-address instructions and 32 one-address instructions. What is the number of zero-address instructions supported by the system ? 5

(b) What is Instruction cycle ? Describe different sub-cycles. Draw the state diagram and explain. 5

5. (a) An instruction is stored at location 300 with address field at location 301. The address field contains 400. A processor register R1 contains 200. Calculate effective address and content of the accumulator if the addressing of the instruction is

(i) Direct (ii) Immediate

(iii) Relative (iv) Indexed with R1 as index register 6

(b) What is RISC architecture? Is it advantageous than CISC ? Justify. 4

6. (a) What do you mean by Virtual memory concept ? How logical address is mapped to physical address ? Explain with example and diagram. 5

(b) What is Cache ? Is it necessary in computer system ? Justify. Explain about write policies of Cache. 5

7. (a) What is Booth multiplication algorithm ? Is it advantageous than general multiplication algorithm ? Justify.

Perform the multiplication step by step 9×-13 using above algorithm. 6

(b) What do you mean by Performance of a system ? How is it measured ? 4

8. Write notes on : 5×2

(a) Hardwired control unit.

(b) Single and Multi bus organization.