Registration No. : | | | | | | | | | | |

Total number of printed pages – 2

B. Tech

BCSE 3309

Fifth Semester (Special) Examination – 2013

COMPUTER ARCHITECTURE AND ORGANIZATION - I

BRANCH : CSE

QUESTION CODE : D304

Full Marks – 70

Time : 3 Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*

The figures in the right-hand margin indicate marks.

1. Answer the following queations : 2×10

   (a) What do you understand by computational models ?

   (b) 64 K memory contains how many words of 8 bits each ?

   (c) The sum of –6 and –13 using 2's complement addition is ?

   (d) What are the different types of fields that are part of an instruction ?

   (e) Distinguish between Pipelining and Replication.

   (f) What are data dependencies between instructions ?

   (g) What is delayed branching ?

   (h) Write the major difference between pipelined processors and superscalar processors.

   (i) What do you understand by The Hypercube ?

   (j) What is software pipelining ?

2. (a) Describe the various levels of abstraction of architecture and computer systems. 5

   (b) What is a Design space ? Explain how do you represent it by DS-trees. 5

P.T.O.

3. (a) Summarize all forms of parallelism that can be exploited at different processing levels of a computer system, including both uniprocessor and multiprocessor approaches. 5

(b) What are the relationship between Languages and parallel architecture ? 5

4. Explain various branch predication schemes with examples. 10

5. (a) Explain the concept of Instruction scheduling in ILP-processors. 5

(b) Write clearly the instruction issue policies of scalar processors. 5

6. (a) What is Register renaming ? Explain with suitable example. 5

(b) Give the pipelined instruction processing in the Pentium. 5

7. (a) Write the principles of VLIW architectures. 5

(b) Describe the various connectivity issues of data-parallel computers. 5

8. Write shorte notes on any **two** of the following. 5×2

(a) Application Scenarious of Pipelines

(b) Instruction Dispatch Scheme

(c) The Recorder Buffer

(d) MIMD Architectures.