Registration no: | | | | | | | | | | |

Total Number of Pages: 02 **B.TECH**
PCCS4301

5TH Semester Regular / Back Examination 2015-16
COMPUTER ORGANIZATION
BRANCH: CIVIL,EEE,FASHION
Time: 3 Hours
Max Marks: 70
Q.CODE: T662

Answer Question No.1 which is compulsory and any five from the rest.
The figures in the right hand margin indicate marks.

Q1 Answer the following questions: **(2 x 10)**

a) What is the difference between valid bit and dirty bit?
b) What is CAM?
c) Differentiate Address space and Memory space by giving example.
d) Write the drawbacks of Programmed I/O and Interrupt driven I/O.
e) Explain Hit-ratio.
f) What is the number of clock cycle necessary to complete 1 fetch cycle in 8085 (including wait state)?
g) Differentiate write-through and write-back.
h) What is the difference system software and application software?
i) Write a program that can evaluate the expression

A x B + C x D

In a single accumulator processor. Assume that the processor has Load, Store, Multiply and Add instructions, and that all values fit in the accumulator.
j) What is Processor Time?

Q2 **a)** Differentiate CISC and RISC. **(5)**
b) Draw the Timing diagram for memory read operation. **(5)**

Q3 **a)** Draw and Explain the hardware implementation of signed magnitude addition and subtraction. **(5)**
b) Explain briefly how data is fetched from memory by giving the instruction set. **(5)**

Q4 What do you mean by Addressing Mode? Explain all types of Addressing Modes with example in each. **(10)**

Q5 **a)** What is Software? Explain different types of software. **(5)**
b) Discuss the operations of DMA. **(5)**

Q6 **a)** Explain the functions of OS. Explain how OS utilizes the resources. **(5)**
b) Explain Direct mapping irrespective of word length. **(5)**

Q7 **a)** Explain briefly one cell of Associative memory with neat diagram. **(5)**
b) Explain the control steps for the instruction Add (R_3), R_1. **(5)**

Q8 Write short notes on any two: **(5 x 2)**
a) Booth Multiplication Algorithm
b) Hardwired control
c) Endian architecture.
d) Types of Bus Structure