Registration no: | | | | | | | | | | |

Total Number of Pages: 02 **B.Tech**
PCCS4301

5th Semester Regular / Back Examination 2016-17
COMPUTER ORGANIZATION
BRANCH(S): CSE, FASHION, FAT, IT, ITE
Time: 3 Hours
Max Marks: 70
Q.CODE:Y458

Answer Question No.1 which is compulsory and any five from the rest.
The figures in the right hand margin indicate marks.

Q1 **Answer the following questions:** **(2 x 10)**

a) What are the basic components according to the von-Neumann architecture?
b) What are the functions of a memory data register and memory address register?
c) The address range of a memory having 7 Addressing lines are from_____H to _____H.
d) What is the function of mode signal for a adder / substractor circuit?
e) What is page replacement algorithm is best and why?
f) What is seek time?
g) What is the use of I/O processor?
h) Why refreshing circuit is required in dynamic RAM?
i) Add 0.2513×10^3 & 0.02513×10^2
j) What is computer architecture?

Q2 **a)** What is computer organization? **(2)**

b) Explain the functional units of a CPU with a suitable diagram? **(8)**

Q3 **a)** Design a memory having FOUR (04) memory chips, each memory chips contains SIXTEEN (16) number of Registers and each register capacity if of 1 byte. **(5)**

b) Explain the instruction execution cycle with state diagram. **(5)**

Q4 **a)** Explain the Addition / Subtraction circuit with a suitable diagram. Find the output of (+45) + (-31) by using that circuit. **(5)**

b) What are the characteristics of a cache? Draw the direct cache having main memory capacity of 24 bytes and cache size of 12 bytes containing each block size of 4 words. **(5)**

Q5 **a)** Explain about the basic organization of micro programmed control unit. **(5)**

How it is advantages over Hardware Control Unit?

b) Explain about the unconditional branch instructions with a suitable example from each. **(5)**

Q6 **a)** Show how the addition operation is performed in a single bus organization, if the operands are available in two CPU registers R1 & R2. **(7)**

b) Write the micro instructions for the above operations. **(3)**

Q7 **a)** Explain about the page replacement algorithm? **(5)**

b) Find out the page fault in FIFO, LRU & optimal page replacement algorithm for the string : 1 2 3 4 1 2 5 1 2 3 4 5 for the page frame size of 3 & 4. **(5)**

Q8 **Write short notes on any two:** **(5 x 2)**

a) Virtual Memory

b) IEEE-488 standard

c) Cache write policies.