210	210	210	210	210	210	210
Regi	stration No :					
Total No	umber of Pages:0	2				3.Tech
210	_		210	210	210 PCS	6D001
210	6 th S	BRAN Max N Time	Back Examin ED SYSTEMS NCH : CSE Marks : 100 : 3 Hours DDE : F900		210	210
Answ	er Question No.1 (F	Part-1) which is co	ompulsory, an n Part-III.		_	Two 210
	The fig	gures in the right	hand margin i	indicate marks) .	
		I	Part- I			
Q1		r Type Questions (A	Answer All-10)			(2 x 10)
a) b) ⁾	Define embedded s	ystems. stand by single functi	ioned system?	210	210	210
c)	•	be performed by follo	•	n :		
d)	Compare between I	RS-232 and RS-485	standards.			
e)	• •	all tasks of RTOS ar				
f)		lows which semapho lices between state c	•			
g) h) ⁾		ciple of abstract leve	210	210	210	
i) j)	•	ent sources of power		MOS circuits?		
			Part- II			
Q2 a)	Explain in detail abo	ort Answer Type Qu out embedded syster	n design flow.	wer Any Eight o	ut of Twelve)	(6 x 8)
b)	Write a note on brai	nch instructions pres	ent in₂ARM.	210	210	210
c) d)	general CPU?	13, R14, and R15. H nunication take place			m counter in a	
e)	Enumerate the structure	·				
f)		tasks be handled in	PMS schedule?	In this context	enumerate the	
210 g)	differencebetween	deferrable and aperion table-driven and cy	odic servers.	210	210	210
h)	Discuss the strategy	y for automated inter	face synthesis.			
i)	Explain the meaning	g of each of the reso	urce constraints	in the ILP-based	d partitioning.	
j)	Construct an examp	ole task set so that it zky's test?	fails Leland's te	est but is still RM	S schedulable.	
k)	What is predictive s system?	hutdown? How does	s it help in impro	oving power perfe	ormance of the	210

210		210	210	210	210	210	210	210					
210	Q3	210	Part-III Only Long Answer Type Questions (Answer Any Two out of Four) Assume that transferring data to/from a register from/to SPI data register in CPU takes 2 ms and in the device 10 ms. Transmission over MOSI/MISO lines is at a rate of 64 Kbps. Compute the time required to transfer 1 Kbyte: (i) from CPU to device, and (ii) from device to CPU. Write a note on Bluetooth Protocol Layers.										
	Q4 What is the role of VHDL in hardware design? Explain in detail about the building blocks of layout.												
210	Q5	210 a) b)	Write a pseudo-code for numbers. Show the corresp What are the different types	onding PRES and	d dual transition r	net models.	of two (8)						
210	Q6	210	Suppose, we have a sequence bit stream. The system our another input 'a' is equal to Draw: a) the FSM for this system b) the StateChart. From this explain how State	tputs '1' wheneve '1', it toggles outp ²¹⁰ and	er the sequence out continually.			21 0					
210		210	210	210	210	210	210	210					
210		210	210	210	210	210	210	210					
210		210	210	210	210	210	210	210					
210		210	210	210	210	210	210	210					