Registration No : | | | | | | | | | | |

Total Number of Pages : 02 **B.Tech**
PET4I104

4th Semester Regular / Back Examination 2018-19
MICROPROCESSOR & MICROCONTROLLER
BRANCH : ECE,ETC
Time : 3 Hours
Max Marks : 100
Q.CODE : F691

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part- I

Q1 **Only Short Answer Type Questions (Answer All-10)** **(2 x 10)**

a) Why a latch is used for an o/p port, but a tristate buffer can be used for an input port?
b) Differentiate between RISC architecture and CISC architecture.
c) What is meant by Wait State?
d) Is there any advantage of two different memories with same effective address? Justify.
e) Write the significance of assembler directives.
f) Distinguish between scanned keyboard code from strobed keyboard code.
g) Give the difference between maskable and non-maskable interrupts.
h) Illustrate the need and role of watch dog timer in 8051.
i) Why SJMP instruction is used in the place of HLT in 8051?
j) State the features of the parallel ports of 8051?

Part- II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 x 8)**

a) "8086 does not directly provide all the signals that are required to control the memory, I/O and interrupt interfaces. Discuss the solution to this issue.
b) Write an 8086 assembly language program to sort the given 10 numbers from memory location 2000H in the ascending order.
c) Explain the interrupt structure of an 8086 microprocessor with its corresponding vector table.
d) Illustrate the memory write and memory read operation in maximum mode of 8086 using timing diagram.
e) Distinguish between the memories mapped I/O and peripheral mapped I/O?
f) What is the purpose of segment registers in 8086 and explain the process control instructions in 8086.
g) Design and explain, the circuit for interfacing of 8086 with 8255 along with the S&H circuit and multiplexor, using appropriate schematic diagram.
h) Describehow 8279 operates for interfacing keyboard to a microprocessor based system?
i) Draw the block diagram of 8279 and describe the section that takes care of data transfer between 8279 and CPU.
j) Find the values of SP (stack pointer) after each of the following instructions

```
MOV SP,#4FH
MOV R1,#30H
MOV R2,#40H
PUSH 1
PUSH 2
MOV R0,#05H
ADD A,R0
POP 2
POP 1
```

k) What is the significance of bit-addressability feature of 8051? Write a program to create a square wave of 50 % duty cycle on bit 0 of port 1.(Use timer 0 , mode 1).

l) Explain with block diagram, how to access external memory device in an 8051 system

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 Draw the interfacing diagram for 8086 based systemfor minimum mode and maximum mode with the following specification. -16 KB RAM -8 KB EPROM -8255 PPI in I/O address space also show the required latches, buffers and decoder. **(16)**

Q4 Discuss in detail the various signal of 8086 and explain in detail about 8086 memory banks and associated signals for byte and word operations. **(16)**

Q5 Sketch the block diagram of 8255(PPI) and explain its various operating modes. **(16)**

Q6 Describe the various modes of operation of Timer/counters in 8051. **(16)**