	Regi	stration No :							
Tota	al Nu	mber of Pages : 02	210	210		210	210	B.Tecl	
Ans	swer	4 <sup>th</sup> Ser Question No.1 (Part	Ma Ti Q	ECTRONIC RANCH: E ax Marks: ime: 3 Hou .CODE: F4	CS CIRCU EE 100 Irs 187	ITS			
		•	res in the rig	Part-III.			_		
		· ·	•	, Part- I	J				
Q1	a) b) 210 c) d) e)	Only Short Answer Type Questions (Answer All-10) What is a single precision-Floating-point representation of numbers? Differentiate between active high and active low terms associated with inputs and							
	f) g) h) i) j)	Among RAM and ROM Write the significance How D/A conversion to Explain the significant Prove the identity, 1+3	M which is wide of Boolean alg takes place? ce of gray and l	ely used in c lebra in digita binary code.	urrent appli al circuits.	ications of da	ata storage?		
Q2	a)	Part- II  Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 x 8)  Explain the operation of a 4-bit SIPO shift register using flip-flops and the timing diagram.  Design a 32:1 MUX using 4:1 MUX(s) only. Mention the LSB and MSB in the diagram.							
	b)	Using NOR gates only	`	,		o anu iviod ii	i tile diagram.		
	c) 210 d) e)	Design a Decade cour Design a 4-bit active necessary circuit.	nter that counts	up.		210 the truth ta	ble. Draw the		
	f) g)	Express the complem $F(A, B, C, D) = \pi(1,5,6)$ Explain the properties	5,7,9,11,12)			t-of-sum form	1.		
	h) 210 i) j)	How will you convert tables and draw the d Given two numbers, A A using 1's compleme Design a 4x3 binary n	iagrams. \= 1110100 an ent method.	d B= 101101		210	210		
	k) I)	Explain the Master-S diagrams. Differentiate between	•	•			cessary circuit		
	210	210	210	210		210	210		

210		210	210	210	210	210	210	210
	Q3	a)	Find all the prime	ver Type Questions (Ansimplicants of the following	g function:	-		(8)
210	F (A, B, C, D) = $\sum$ (0,2,4,5,6,7,8,10,13,15). Mention all the desired minimizations Minimize the function: F (w,x,y,z) = $\sum$ (4,5,6,7,12,13,14), d (w,x,y,z) = $\sum$ (1,9,11,15)							
	Q4		flop. Consider the	down asynchronous cour two asynchronous input ary tables and final circuit	ts and a syn	negative edge-trigg chronous clock. D	gered JK flip- raw the state	(16)
210	Q5			c, implement the function xplain the operation.	F (A, B, C) =	= (A+B). (B+C). (A+	-C). Draw the	<b>(16)</b> 210
				nd D/A conversion. reen PAL and PLA.				(10) (6)
210		210	210	210	210	210	210	210
210		210	210	210	210	210	210	210
210		210	210	210	210	210	210	210
210		210	210	210	210	210	210	210
210		210	210	210	210	210	210	210