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Total Number of Pages : 01

B.Tech
PCEC4202

4thSemester Back Examination 2018-19

DIGITAL ELECTRONICS CIRCUIT

BRANCH : AEIE, BIOMED, CSE, ECE, EEE, EIE, ETC, IEE, IT, ITE

Time : 3 Hours

Max Marks : 70

Q.CODE : F203

Answer Question No.1 which is compulsory and any five from the rest.
The figures in the right hand margin indicate marks.

Q1 Answer the following questions : (2 x 10)

- What do you understand by "cell adjacency" in K-map?
- Write the applications of state machines.
- How "fan-in" and "fan-out" are different from each other?
- Draw the block diagram for construction of a full adder using half-adders.
- Convert $(306.D)_{16}$ to $()_2$.
- How sequential circuits are analyzed using the number of states?
- State the basic MOSFET design rules in VLSI.
- Write a module for a full adder in VHDL.
- What are the libraries used in VHDL?
- Between 1's and 2's complement methods of number representation, which is more preferred and why?

Q2 a) Write the steps for designing any function using only NOR gates. Explain with an example. (5)

b) Differentiate between decoders and demultiplexers. Under what circumstances a decoder can be converted to a demultiplexer? (5)

Q3 a) Simplify the following Boolean function using four-variable K-map to SoP form. (5)

$$F(w, x, y, z) = \sum(1, 4, 5, 6, 12, 13, 14, 15)$$

b) Differentiate between RAM and ROM. (5)

Q4 a) Reduce the function $F(A, B, C) = A'C' + ABC + AC' + AB'$ to two literals. (5)

b) Differentiate between sequential circuit and combinational circuits. (5)

Q5 a) Design a binary multiplier for multiplying two 2-bit binary numbers. (5)

b) Design a NOT gate using CMOS logic. (5)

Q6 Design a 4-bit up/down counter using a negative edge triggered T flip-flop. The clock is applied in an asynchronous manner. (10)

Q7 Describe the evolution of VLSI along with the "patterning" and "lithography" techniques. (10)

Q8 Write short answer on any TWO : (5 x 2)

a) Floating-point number representation

b) CMOS memories

c) Hardware Description Language