Registration No : | | | | | | | | | | |

Total Number of Pages : 02 **B.Tech**
PCS4I101

4th Semester Regular / Back Examination 2018-19
COMPUTER ORGANIZATION & ARCHITECTURE
BRANCH : CSE
Max Marks : 100
Time : 3 Hours
Q.CODE : F254

Answer Question No.1 (Part-1) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.
The figures in the right hand margin indicate marks.

Part- I

Q1 Only Short Answer Type Questions (Answer All-10) **(2 x 10)**

a) The main memory of personal computer is made up of _____.
b) What are the steps involved in an instruction cycle?
c) In which addressing mode, the operand is given explicitly in the instruction?
d) State some of the common rules of assembly language?
e) Status bit is also called _____.
f) What is it so called, the average time required to reach a storage location in memory and obtained its content?
g) State SIMD representation.
h) Write the basic components in a microprocessor?
i) Define vertical micro code, explain the designing strategy of a control unit coded on vertical code?
j) Suppose the cpu is busy but you want to stop and do some other task. How do you do it?

Part- II

Q2 Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) **(6 x 8)**

a) Write a program that can evaluate the expression : (A*B)+(C*D)+(E*F) in a single accumulator processor.
b) Justify Briefly About Flip-flops with design?
c) Illustrate the requirement of page-table and the different ways in which the table can be organized.
d) Analyze the partitioning technique in reference to memory systems? Give their advantages and disadvantages?
e) Briefly explain the two hardware methods to establish priority?
f) Registers R1,R2 of a computer contain the decimal values 1100 & 3400. What is the effective address of the memory command in each of the instructions:
   a. Store R4,10(R2)
   b. Move #1000,R7
   c. Load 14(R1),R3
   d. Add (R1)+,R4
   e. R3,25(R1,R2)
g) What are the major difficulties of pipeline conflicts in processors supporting pipe lining?
h) Explain what are the different hazards? How do we avoid them?
i) Develop the two hardware methods to establish priority?
j) Design Flynn's classification of computers.
k) Using Booth's multiplication algorithm perform the operation A * B where A and B are the signed 2's compliment numbers.

A=010111, B=110110

l) Distinguish between RISC and CISC instructions structure.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 How DMA (Direct Memory Access) controller works ? Explain with diagram. **(16)**

Q4 Minimize and solve the expression using 4 variable K-Map. **(16)**
F(x)=m(0,1,2,3,4,6,7,9,11,12,14,15). Design the circuit diagram of the expression using universal logic OR & AND gates.

Q5 How can you calculate the performance of memory? Explain cache1, cache2 with an example. A computer has a 256 KByte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit. Find out the number of bits in the tag field of an address? **(16)**

Q6 Give briefly structure of the various levels of RAID structure. **(16)**