Registration No: | | | | | | | | | | |

Total Number of Pages: 02 **B.Tech.**
PET5H002

5th Semester Regular Examination 2017-18
Digital VLSI Design
BRANCH: ECE, ETC
Time: 3 Hours
Max Marks: 100
Q.CODE: B452

Answer Question No.1 and 2 which are compulsory and any four from the rest.
The figures in the right hand margin indicate marks.

Q1 **Answer the following questions: *multiple type or dash fill up type*** **(2 x 10)**

a) What do you mean by fan out of a logic gate?
   a. The same amount of cooling required by a gate.
   b. The physical distance between the output pins on device.
   c. Number of other gates that can be connected to gate output.
   d. Number of other gates that can be connected to gate input.

b) Silicon dioxide layer is used
   a. To protect the surface.
   b. It acts as barrier to dopant.
   c. It acts as insulating substrate.
   d. All of above.

c) The threshold voltage is defined as
   a. The work function difference between gate and channel.
   b. Gate voltage component to change surface potential.
   c. Gate voltage to offset depletion region charge.
   d. All of above.

d) In n-channel mosfet transistor
   a. The source is at higher potential than drain.
   b. The source is at lower potential than drain.
   c. The source is at same potential than drain.
   d. None of the above

e) CMOS technology is better than bipolar technology because of,
   a. Its high noise margin.
   b. Its low packing density.
   c. Its low input impedance.
   d. None of above.

f) What do you mean by the rise time of a waveform,
   a. Time delay from when the input step changes by 50% to when the output step changes by 50%.
   b. Time taken for the waveform to decrease from 90% to 10% of its value.
   c. Time taken for the waveform to increase from 10% to 90% of its value.
   d. Time taken for the waveform to increase from 50% to 100% of its value.

g) nMos pass transistor can pass a _____ '0' signal.
h) Elmore delay is used for measuring _____.
i) Stuck at faults occur when a line is permanently stuck to _____.
j) FPGA stands for _____.

Q2 **Answer the following questions: *Short answer type*** **(2 x 10)**

a) What do you understand by Local Oxidation of LOCOS.
b) What are the main parameters to be taken care of while designing any VLSI chip in general?
c) Draw y=a'.b.c+c.d using CMOS design style.
d) What do you understand by Inversion Layer?
e) Draw the VTC of a CMOS inverter with proper labeling.
f) What do you understand by static and dynamic power.
g) What is the difference between combinational & sequential MOS circuits?
h) What is the need of testing a VLSI chip.
i) Which memory is fastest in operation?
j) What do you understand by a floating gate.

Q3 **a)** Explain in detail VLSI design flow through Y-chart. **(10)**
b) Describe the terms Regularity, Modularity and Locality. **(5)**

Q4 **a)** Draw the fabrication steps for a CMOS device making process. **(10)**
b) Write a note on Computer Aided Design Technology. **(5)**

Q5 **a)** How does a MOS system will behave under external bias. Describe with the help of diagrams in regard to band diagram. **(10)**
b) Considering the MOS structure made of a p-type silicon substrate, a SiO_2 layer, and a aluminum gate. The equilibrium Fermi potential of the doped silicon substrate is given as $q.\Phi_{Fp}$ = 0.2 eV. Using the electron affinity value for silicon as 0.95 eV and the work function for aluminum as 4.1 eV. Calculate the built-in potential difference across the MOS system. Assume that the MOS system contains no other charges in the oxide or on the silicon-oxide interface. **(5)**

Q6 **a)** Derive the I-V equations for a nMOS for different regions of operation. **(10)**
b) Write a note on scan-based techniques for VLSItesting. **(5)**

Q7 **a)** Draw CMOS circuit diagram, stick diagram and layout diagram for a NOR2 gate with proper explanation. **(10)**
b) Differentiate between inverters with enhancement type nMOS load and depletion type nMOS load. **(5)**

Q8 **a)** Draw a 4:1 MUX using transmission gate logic. Compare it with its pass transistor counterpart. **(10)**
b) Explain about DRAM with proper diagram. **(5)**

Q9 **a)** Draw a neat and complete diagram for a 6 cell SRAM. Explain its operation in detail. **(10)**
b) Draw a 2 input Ex-OR gate using pass transistor logic. **(5)**