Registration No. :

Total number of printed pages – 3

B. Tech

PCEC4201

Third Semester (Back / Special) Examination – 2013

ANALOG ELECTRONICS CIRCUITS

BRANCH : AEIE, BIOMED, CSE, EC, EEE, ELECTRICAL, ETC, IEE, IT

QUESTION CODE : D 217

Full Marks – 70

Time : 3 Hours

Answer Question No. *1* which is compulsory and any **five** from the rest.
The figures in the right-hand margin indicate marks.

1. Answer the following questions :   2 ×10

    (a) What is dynamic resistance of a diode? How it is evaluated numerically ?

    (b) Three OPAMP based instrumentation amplifiers are better than single OPAMP
         based instrumentation amplifiers. Justify.

    (c) How does base resistor (RB) affect the input resistance of a CE amplifier ?
         Justify

    (d) What are the small signal h-parameters that are determined from input
         characteristics of a transistor amplifier ?

    (e) Why wein bridge oscillators are most popular in audio frequency range ?

    (f) What are two salient features of a 'buffer amplifier' ?

    (g) What is the bandwidth of the amplifier when the rise time is 0.1 msec ?
         What should be the rise time of an ideal voltage amplifier ?

    (h) What is CMRR of an OPAMP ? How CMRR can be increased during the
         manufacturing of OPAMP ?

P.T.O.

(i) What is pinch-off voltage of FET ? Why drain current is almost constant when source-drain voltage exceeds pinch-off voltage ?

(j) Why a constant current source is used in place of R_E in the differential amplifier stage of the OPAMP ?

2. (a) Draw a self bias circuit of transistor amplifier. Then, find the load line and operating point (I_{CQ}, V_{CEQ}) of the above transistor amplifier in terms of its circuit components.　　　　5

(b) Derive an expression for the overall bandwidth when N no. of identical voltage amplifiers is connected in cascade.　　　　5

3. (a) Explain the odd harmonic cancellation property of a push pull power amplifier. Justify your answer mathematically.　　　　5

(b) Explain the principle operation of a push pull power amplifier. Compare its performance with Complementary symmetry power amplifier.　　　　5

4. (a) Derive the condition for oscillation in RC phase shift oscillator.　　　　5

(b) Derive the input impedance (Z_i) and output impedance (Z_O) of a unit feedback voltage series–ve feedback amplifier in terms of its open loop parameters.　　　　5

5. (a) Draw a voltage divider bias emitter follower circuit. Draw its r_e equivalent circuit. Derive its voltage gain. What is its importance in analog circuits ?　　　　5

(b) Design a 1st order active low pass filter which have gain = 5 and cut-off frequency 5 KHz. Suggest, how the bandwidth of the can be improved without increasing the rise time of the circuit.　　　　5

6. (a) A FET amplifier in common-source configuration uses a load resistance of 250 KΩ. The ac drain resistance of the device is 100 KΩ and the transconductance is 0.5 mA/V. Calculate the voltage gain and the output resistance of the amplifier.　　　　5

(b) The voltage gain of a transistor amplifier is 50. Its input and resistances are 1 KΩ and 40 KΩ. If the amplifier is provided with 10% negative voltage feedback in series with the input, calculate the closed loop voltage gain, input resistance and output resistance. 5

7. (a) Draw a three OPAMP based instrumentation amplifier circuits and Derive its voltage gain in terms of circuit components. Mention its applications. 5

(b) Design a OPAMP based analog circuits which will give an output voltage, $V_0 = 0.5 V_1 - 2 V_2 + 0.25 V_3$, Where, V_1, V_2 and V_3 are three input voltages. 5

5×2

8. Write short notes on any **two** of the following :

(a) Stability of transistor Biasing

(b) Cascode amplifiers

(c) Current mirror circuit

(d) Miller effect capacitance.