GIET MAIN CAMPUS AUTONOMOUS GUNUPUR – 765022

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4th Semester Regular Examination-April-May 2019

BECPC 4010 – DIGITAL ELECTRONICS

(Regulations 2017) Common to AEIE / ECE Branch

Time : 3 Hours Maximum : 100 Marks

Answer ALL Questions

The figures in the right hand margin indicate marks.

PART – A: (Multiple Choice Questions) 10 x 2=20 Mark

Q.1. Answer *All* Questions.

a An example of a self-complementing code is [CO1] [PO1]
(a.) 8421 code (b.) 7421 code (c) excess-3-code (d) gray code

b The Boolean expression: $ABC + \bar{A}\,\bar{B}\,C + AB\bar{C} + \bar{A}\bar{B}\bar{C}$ [CO1] [PO1]
a) OR Gate (b) AND gate (c) EX-NOR gate (d) EX-OR gate

c The POS form of expression is suitable for circuit using [CO1] [PO1]
a) XOR b). NAND c). AND d).NOR

d What is the number of selection line required in 1× N demultiplexer? [CO2] [PO1]
a) 2 b) n c) 2^N d) $\log_2 N$

e D flip-flop can be made from a J-K flip-flop by making [CO3] [PO1]
a) J=K b) J = K = 1 c) J = 0, K = 1 d) J = $\overline{K}$

f In Schottky TTL, a Schottky diode is used for [CO3] [PO1]
a) Forming the gate b) Connecting the resistor c) Clamping of the base collector junction d) None of these

g A 4-bit module- 16 ripple counter uses J-K flip-flop. If the propagation delay of each flip-flop is 50 ns, the maximum clock frequency that can be used is equal to [CO3] [PO1]
a) 20 MHz b) 10 MHz c) 8 MHz d) 5 MHz

h Extremely low power dissipation and low cost per gate can be achieved in the following: [CO4] [PO1]
a) ECL b) CMOS c) TTL d) MOS

i What are the minimum number of 2-to-1 multiplexers required to generate a 2-input AND gate and a 2-input Ex-OR gate? [CO2] [PO1]
a) 1 and 2 b) 1 and 3 c) 1 and 1 d) 2 and 2

j A square wave with a period of 10 μs drives a T flip-flop. The period of the output signal will be: a)100 μs b) 20 μs c) 10 μs d) 5 ms [CO4] [PO1]

PART – B: (Short Answer Questions) 2x10=20 Marks

Q.2. Answer *ALL* questions

a Design a modulo 8 counter using D flip flop in state machine approach. [CO3] [PO1]

b Draw the logic circuit of a half subtractor. [CO4] [PO1]

c Mention the advantages of JK-FF over SR-FF. [CO2] [PO1]

d An 8-bit DAC has a step size of 5 mV. Determine the full-scale output voltage and the percentage resolution. [CO2] [PO2]

e What is De Morgan's theorem? [CO2] [PO1]

f Discuss the properties of excess-3 code. [CO4] [PO1]

g Convert $(806.25)_{10} = (?)_2$ [CO4] [PO2]

h Differentiate between PLA and PAL. [CO4] [PO1]

i What is race around? Explain don't care condition. [CO4] [PO1]

j Explain R-2R ladder? [CO4] [PO1]

PART – C: (Long Answer Questions) 15x4=60 Marks

Q.3 Answer *ALL* questions

a. Simplify the given Boolean function using Quitne-McClusky method: $Y=f(a, b, c, d)=\sum(0, 2, 3, 5, 8, 10, 11)$ Verify the results using k-map. — 12 Marks — [CO1] [PO2]

b. Distinguish between prime implicant and essential prime implicant — 3 Marks — [CO1] [PO1]

OR

c. On an examination, a student wrote $(2756)_6$ as the answer to a question. Since 7 and 6 are greater than 5, the largest digit permitted in the radix 6 system, the answer must be wrong. What would you guess is the most likely decimal equivalent of this number, and why? — 3 Marks — [CO1] [PO2]

d. Find a minimal sum for following Boolean function using decimal QM method and PI table reduction. — 12 Marks — [CO1] [PO2]

$$f(a, b, c, d) = \sum m\,(1,3,6,8,9,10,12,14) + d(7,13)$$

Q.4

a. Implement the following Boolean function using 8:1 multiplexer: $Y = f(a, b, c, d) = \bar{A}\,B\bar{D} + ACD + \bar{B}CD + \bar{A}\bar{C}D$ — 9 Marks — [CO2] [PO1]

b. Define decoder Implement the following multiple output function using IC74138 and external gates. Also write the truth table. — 6 marks — [CO2] [PO2]

$P=f_1(X, Y, Z)=\sum(1, 2, 5, 6)$

$P=f_1(X, Y, Z)=\prod(3, 5, 6, 7)$

OR

c. What is a magnitude comparator? Design a two-bit digital comparator by writing TT, relevant expressions and logic diagram. — 10 Marks — [CO2] [PO1]

d. Implement the following function using single 3:8 decoder $F(a, b, c)=\prod(1, 3, 5, 7)$. — 5 Marks — [CO2] [PO2]

Q.5

a. What is flip-flop. Discuss working principle of JK flip-flop with its TT. — 7 Marks — [CO3] [PO1]

b. What is significance of edge triggering? Explain working of positive edge triggered D flip-flop with their functional table. — 8 Marks — [CO3] [PO1]

OR

c. Explain PIPO and SIPO operations using single diagram. — 6 Marks — [CO3] [PO2]

d. Design Mod-6 synchronous counter using JK flip-flop. The sequence is 000, 001, 011, 100, 101, 111…000. — 9 Marks — [CO3] [PO2]

Write state diagram for Mod-5 self-correcting counter and briefly explain. — [CO] [PO1]

Q.6

a. Which type of A/D converter is faster and explain it briefly. — 5 Marks — [CO4] [PO1]

b. Which type of A/D converter is accurate and explain it briefly. — 10Marks — [CO4] [PO1]

Compare ROM and RAM.

OR

c. Draw an inverter in RTL, DTL, ECL, TTL and CMOS logic circuits. — 10 Marks — [CO4] [PO1]

d. Explain briefly about Programmable Logic Array. — 5 Marks — [CO4] [PO1]

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