Registration No: | | | | | | | | | | |

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B.TECH
PEL3I102

3rd Semester Regular Examination 2016-17
ANALOG ELECTRONICS CIRCUITS
BRANCH: EEE
Time: 3 Hours
Max Marks: 100
Q.CODE: Y479
Answer Part-A which is compulsory and any four from Part-B.
The figures in the right hand margin indicate marks.

Part – A (Answer all the questions)

Q1 Answer the following questions: *multiple type or dash fill up type* **(2 x 10)**

a) The early effect of bipolar junction transistor is caused by
1) Fast turn on 2) Fast turn off 3) Large collector-base reverse bias 4)Large emitter-base forward bias.

b) A differential amplifier has a differential gain of 20,000. CMRR = 80db. The common mode gain is given by
(1) 1 (2) 0.5 (3) 2 (4) 0

c) In a CB amplifier the maximum efficiency could be
a) 99 % b) 85% c) 50% d) 25%

d) The horizontal intercepts of dc load line is the same as ideal
a) Cut-off point b) Saturation point c) Operating point
b) Quasi saturation point.

e) Generally the gain of a transistor amplifier falls at high frequencies due to the a)Internal capacitance of the device (b)coupling capacitor at the input (c) skin effect (d) coupling capacitor at the output

f) An ideal op-amp is an ideal
a)current controlled current source (b)current controlled voltage source (c)voltage controlled voltage source(d)voltage controlled current source

g) What should be the value of unity gain frequency for a short circuit CE transistor with gain of 30 at 4MHz and cut-off frequency of about 100 kHz? (a)40MHz (b)80MHz(c)120MHz(d)150MHz

h) The rate of -20 dB/decade is almost equivalent to _____
a. -4 dB/octave b. -6 dB/octave c. -8 dB/octave d. -10 dB/octave

i) Which among the below mentioned implementation strategies is/are precise to obtain an AC equivalent circuit of MOSFET?
(a) Replacement of all capacitors by open circuits
(b) Replacement of all capacitors by short circuits
(c) Setting of all DC voltages to zero
(d) Setting of all DC voltages to unity

j) Why is the practical value of | Aβ | considered or adjusted to be slightly greater than '1'?

(a) To compensate for noise voltage(**b)**To compensate for phase shifting of two relevant signals upto 180°(**c)** To compensate for non-linearities existing in the circuit(**d)** To compensate for the change in feedback voltage

Q2 **Answer the following questions: *Short answer type*** **(2 x 10)**

a) Why it is necessary to provide proper dc biasing to a transistor?
b) Differentiate between cut-off Frequency and Unity-gain frequency?
c) Four identical amplifiers are connected in cascade. Each one has upper cut off frequency of 40KHz.find out the overall bandwidth of the cascade.
d) Derive an expression for total collector current in CE configuration.
e) What is CMRR and Slew-rate.
f) For a fixed bias configuration by using BJT, Vcc=+9v,&Rc=1.8KΩ.Draw the Load line and find Ic(max).
g) Define Threshold voltage for a MOSFET.
h) What are the minimum values of gain in inverting and non-inverting amplifiers?
i) Why is the Darlington configuration not suitable for more than two transistors?
j) Differentiate between BJT and FET.

Part – B (Answer any four questions)

Q3 **a)** Derive an expression for the voltage gain of an instrumentation amplifier. What are its applications? What is the need of current mirror circuit? Draw one circuit. **(10)**

b) Explain the frequency response of an op-amp. **(5)**

Q4 **a)** What is stability factor? write the general expression for S(ico) and S(β). **(10)**

b) Calculate the gain, input and output impedance of a voltage series feedback amplifier A= -300, R_i = 1.5 kilo-ohms, R_o= 50 kilo-ohms, and β= -1/15. **(5)**

Q5 **a)** Sketch the CE hybrid equipment model, given $I_{E(dc)}$ = 1.2mA, Beta= 120, and r_0 =40k-ohms. **(10)**

Sketch the re model for CE transistor amplifier. Determine the following if beta=80, $I_{E(dc)}$ = 2mA and r_0 =40k-ohms.
i) Zi ii) Ib iii) Ai if RL =1.2k-ohms iv) Av if RL= 1.2k-ohms.

b) Explain frequency response of BJT amplifiers**.** **(5)**

Q6 **a)** Briefly explain the principle and operation of N-channel and P-channel MOSFET with its transfer characteristics. **(10)**

b) Show that transconductance "g_m" of a JFET is related to the drain current I_{ds} by ; $g_m = \frac{2}{|V_P|}\sqrt{I_{DSS} \times I_{DS}}$ **(5)**

Q7 **a)** Draw an emitter follower of source follower circuit?(i)what is the type of feedback(ii)find the feedback Factor(iii)find the voltage gain with and without feedback. How are the input and output impedances affected by feedback? **(10)**

b) Draw and analyze a D-MOSFET configuration. why is it called so? **(5)**

Q8 **a)** Explain the principle of operation of crystal oscillator. Draw the frequency response of crystal oscillator. **(10)**

b) Derive the expression for an integrator circuit by using op-amp? **(5)**

Q9 **a)** For the voltage divider JFET network,(a) sketch the two port model by calculating A_{VNL}, Zi and Z_0 (b) Using system approach determine Av and Avs. **(10)**

b) Show that rise time of a single stage amplifier is proportional to its upper 3dB cutoff frequency. **(5)**