Registration No: | | | | | | | | | | |

Total Number of Pages: 03 **B.TECH**

PET3I104

3rd Semester Regular Examination 2016-17

DIGITAL ELECTRONICS

BRANCH: ECE, ETC

Time: 3 Hours

Max Marks: 100

Q.CODE:Y530

Answer Part-A which is compulsory and any four from Part-B.

The figures in the right hand margin indicate marks.

Part – A (Answer all the questions)

Q1 **Answer the following questions:** **(2 x 10)**

a) The decimal equivalent of Binary number 11010 is
(A) 26 (B) 36 (C) 16 (D) 23

b) -8 is equal to signed binary number
(A) 10001000 (B) 00001000 (C) 10000000 (D) 11000000

c) Pick the correct choice: $x + xy =$
(A) x(B) y(C)1(D) 0

d) Which of the following is the fastest logic
(A) TTL **(B)** ECL **(C)** CMOS **(D)** LSI

e) The device which changes from serial data to parallel data is
(A) COUNTER (B) MULTIPLEXER (C) DEMULTIPLEXER (D) FLIP-FLOP

f) A ring counter consisting of five Flip-Flops will have
(A) 5 states **(B)** 10 states **(C)** 32 states **(D)** Infinite states.

g) Each Flip-flop stores ---------- bit(s)
A. 1 bit B. 8 bit C. 16 bit D. 2 bit

h) State True or False: Excess-3 is a reflective code.

i) State True or False: EPROM contents can be erased by exposing it to X-Rays

j) State True or False: The output of a logic gate is 1 when all its inputs are at logic 0. The gate is either a NOR or an EX-NOR.

Q2 **Answer the following questions:** **(2 x 10)**

a) Using 10's complement, subtract 72532 - 3250.

b) Find the Unknown base $(240)_{10}=(1430)_x$

c) Show that the dual of the exclusive-OR is equal to its complement.

d) Write the following Boolean expressions in sum of products form:
$$Y = (B + D)(A' + B' + C)$$

e) Prove the Distributive property of Boolean Algebra.

f) Draw a 2 bit by 2 bit Binary Multiplier circuit.

g) What is the maximum positive and maximum negative number that can be represented by a 4 bit binary number using-
(i) 1's Complement notation. (ii) 2's Complement notation.

h) Why a pulse transition circuit is used in the clock circuit of an edge triggered JK Flip Flop.?

i) Fill up the last Column of the following table for a SR Latch with control:

En	S	R	Next State of Q
0	X	X	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

j) What is a PAL? Give an example.

Part – B (Answer any four questions)

Q3 **a)** Simplify the following Boolean functions *T*1 and *T*2 to a minimum number of literals: **(10)**

A	B	C	*T*1	*T*2
0	0	0	1	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	0	1

b) Express the following Boolean function as a product of maxterms. **(5)**

$$F = xy + x'z$$

Q4 **a)** Minimize and design the function f(A,B,C,D)=Σ(0,1,3,5,7,8,9,10,11,12,14) using K-map. Find all the prime implicants and essential prime implicants. **(10)**

b) What do you mean by positive logic and negative logic? Show that a positive logic NAND gate is a negative logic NOR gate and vice versa. **(5)**

Q5 **a)** Twelve months of a calendar are represented by a 4 bit binary representation, where 0010 represents January, 0011 represents February and so on. Design a switching circuit which will light up an LED when fed with the 4 bit input pattern corresponding to a month having 31 days. Use minimum number of NAND gates. **(10)**

b) Convert : **(5)**

(i) $(10110.0101)_2 \rightarrow (\quad)_{10}$

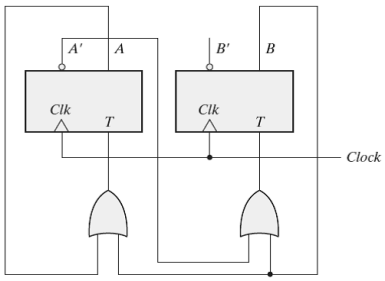
(ii) $(F00D)_{16} \rightarrow (\quad)_2$

(iii) $(1001001.01)_8 \rightarrow (\quad)_{16}$

(iv) $(365)_{10} \rightarrow (\quad)_8$

(v) $(1111101111011110)_2 \rightarrow (\quad)_{16}$

Q6 **a)** Derive the state table and the state diagram of the sequential circuit shown in Figure below. **(10)**



b) (i) Convert $(10110)_2$ to Gray code. **(5)**

(ii) Simplify the expression using Boolean algebra.

$$F=\overline{\overline{A\bar{B}} + \overline{ABC}} + A(B + \overline{A\bar{B}})$$

Q7 **a)** Draw the state diagram of a MOD-3 counter. Write its excitation table and draw the circuit diagram of a MOD 3 synchronous counter using JK Flip Flops. **(10)**

b) Design a shift left SISO register using D Flip Flops. Show how a pulse 0101 is shifted using this type of register. **(5)**

Q8 **a)** Draw the circuit diagram of a Master-slave J-K flip-flop using NAND gates. What is race around condition? How is it eliminated in a Master-slave J-K flip-flop? **(10)**

b) Write a short note on PROM. **(5)**

Q9 **a)** Design a combinational circuit that gives a binary output equal to the square of binary-coded decimal numbers 0 through 9 using ROM. **(10)**

b) Implement a two input NAND and a two input NOR gate using the following logic styles **(5)**

(i) DTL logic

(ii) CMOS Logic.