Registra	ation No:	
Total No	umber of Pages: 02 210 210 210 2	B.TECH 21 PCS3I101
3 rd Semester Regular Examination 2016-17 Switching Theory and Logic Design BRANCH: CSE		
210	Time: 3 Hours 210 Max Marks: 100 210 210	10 21
Q.CODE: Y505 Answer Part-A which is compulsory and any four from Part-B. The figures in the right hand margin indicate marks.		
Q1 a) b)	Radix of binary number system is? In the gray code, each successive code differs from its preceding code	(2 x 10) ₂₁
c) d)	(i) Minimal (ii) Irredundant (iii) Both(i) or (ii) (iv) None 1+A+AB+ABC+ =	
e) 210 f)	(i) Is faster (iii) is more accurate (ii) uses fewer gate (iv) cost less	10 21
h) i)	Flip flop is widely used for data storage purpose. The bit sequence 1010 is serially entered (right-most bit first) into a 4 bit parallel out shift register that is initially clear. What are the Q output after two clock pulses? (i) 0011 (ii) 1001 (iii) 1111 (iv)1000 The frequency at the MSB of a MOD-8 counter, clocked by 20 KH	S 21
Q2 ₂₁₀ a)	Answer the following questions: Determine the base of the number if 24+17=40.	(2 x 10)
210 a) b) c) d) e)	Convert $(41.6875)_{10}$ into binary number. Find the complement and dual of the expression. $F = x(y'z'+yz)$. What is prime implicant in K-Map? When it is said to be essential? How can a decoder be used as demultiplexer?	10 21
f) g) h)	What is meant by priority encoder? How is it different from encoder? How a D-flip flop obtained from JK flip flop? Write its truth table. What is meant by storage capacity of a register?	10 21

When two states are said to be equivalent?

Part – B (Answer any four questions) Q3 a) Briefly explain about error detection and correction code. A transmitter (10)uses a single error correcting code for the message using even parity. The message received at the receiving end is 1110101. Check and correct the error. b) Add the two numbers (-12, +7) using both 1's and 2's complement (5) Method. Simplify the Boolean expression by using Quine-Mc Clusky Method. (10) $F(A,B,C,D) = \sum m(0,1,3,5,7,8,9,10,13,15)$ Simplify the following function using 4-variable K-Map and draw the (5) simplified logic circuit using universal gate. $F(A, B, C, D) = \sum m(1, 3, 4, 5, 8, 10, 11, 15) + \sum d(0, 2, 7, 14)$ Implement the Boolean function using Multiplexer and suitable gates. Q5 (10) $F(A,B,C,D) = \sum m(1,3,4,6,7,9,11,14)$ 16×1 MUX (ii) 8×1 MUX (iii) 4×1 MUX (i) (iv) 2×1 **b)** Construct a 4 to 16 line decoder using five 2×4 decoder with enable. (5) Q6 A PN Flip flop has four operations: clear to 0, No change, Complement (10)and Set to 1, when inputs P and N are 00, 01, 10 and 11 respectively. (i) Tabulate the characteristic table (ii) Derive the characteristics Equation (iii)Tabulate the excitation table (iv) Show how the PN flip flop can be converted to a D-flip flop. b) Show that how a T-flip flop used as a divided-by-2 element. Explain (5) with proper waveform. Differentiate between synchronous and Asynchronous counter. Draw (10)Q7 a) the state diagram of 4-bit decimal counter. Draw an Asynchronous decimal counter using any suitable flip flops and compare with a synchronous decimal counter. b) What is a Shift Register? How many types are there? Explain the (5) principle of parallel in serial out shift register. Q8 a) A sequential circuit with two D flip flops, A and B; two inputs x and y; (10)and one output z is specified by the following next state and output equations: Z = BA(t+1) = x'y + xA, B(t+1) = x'B + xA, (i) Draw the logic diagram of the circuit (ii) List the stable for the sequential circuit (iii) Draw the corresponding state diagram. (iv) Using this state equation design the circuit with JK flip flop. b) Explain about Algorithmic State Machine (ASM). Draw the ASM chart of (5) a Modulo-4 UP/Down Counter. Q9 a) Write Short Notes on: (10)(i) Magnitude Comparator (ii) Ring Counter b) Design a combinational circuit whose output is equal to 1 if the input (5) variable has more 1's than 0's. Otherwise the output is 0. Design a 3

input majority circuit.

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